SILICON TERAHERTZ ELECTRONICS: CIRCUITS AND SYSTEMS FOR FUTURE APPLICATIONS

A Dissertation

Presented to the Faculty of the Graduate School

of Cornell University

in Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy

by

Chen Jiang

May 2018

SILICON TERAHERTZ ELECTRONICS:

CIRCUITS AND SYSTEMS FOR FUTURE APPLICATIONS

Chen Jiang, Ph.D.

Cornell University 2018

The terahertz frequency bands are gaining increasing attention these days for the potential applications in imaging, sensing, spectroscopy, and communication. These applications can be used in a wide range of fields, such as military, security, biomedical analysis, material science, astronomy, etc. Unfortunately, utilizing these frequency bands is very challenging due to the notorious "terahertz gap". Consequently, current terahertz systems are very bulky and expensive, sometimes even require cryogenic conditions. Silicon terahertz electronics now becomes very attractive, since it can achieve significantly lower cost and make portable consumer terahertz devices feasible. However, due to the limited device f_{max} and low breakdown voltage, signal generation and processing on silicon platform in this frequency range is challenging.

This thesis aims to tackle these challenges and implement high-performance terahertz systems. First of all, the devices are investigated under the terahertz frequency range and optimum termination conditions for maximizing the efficacy of the devices is derived. Then, novel passive surrounding networks are designed to provide the devices with the optimal termination conditions to push the performances of the terahertz circuit blocks. Finally, the high-performance circuit blocks are used to build terahertz systems, and system-level innovations are also proposed to push the state of the art forward.

In Chapter 2, using a device-centric bottom-up design method, a 210-GHz

harmonic oscillator is designed. With the parasitic tuning mechanism, a wide frequency tuning range is achieved without using lossy varactors. A passive network based on the return-path gap coupler and self-feeding structure is also designed to provide optimal terminations for the active devices to maximize the harmonic power generation. Fabricated with a 0.13-μm SiGe BiCMOS process, the oscillator is highly compact with a core size of only 290×95 μm^2. The output frequency can be tuned from 197.5 GHz to 219.7 GHz, which is around 10.6% compared to the center frequency. It also achieves a peak output power and dc-to-RF efficiency of 1.4 dBm and 2.4%, respectively. The measured output phase noise at 1 MHz offset is -87.5 dBc/Hz. The high power, wide tuning range, low phase noise, as well as compact size, make this oscillator very suitable for terahertz systems integration.

In Chapter 3, the design of a 320-GHz fully-integrated terahertz imaging system is described. The system is composed of a phase-locked high-power transmitter and a coherent high-sensitivity subharmonic-mixing receiver, which are fabricated using a 0.13-μm SiGe BiCMOS technology. To enhance the imaging sensitivity, a heterodyne coherent detection scheme is utilized. To obtain frequency coherency, fully-integrated phase-locked loops are implemented on both the transmitter and receiver chips. According to the measurement, consuming a total dc power of 605 mW, the transmitter chip achieves a peak radiated power of 2 mW and a peak EIRP of 21.1 dBm. The receiver chip achieves an equivalent incoherent responsivity of more than 7.26 MV/W and a sensitivity of 70.1 pW under an integration bandwidth of 1 kHz, with a total dc power consumption of 117 mW. The achieved sensitivity with this proposed coherent imaging transceiver is around ten times better compared with other state-of-the-art incoherent imagers.

In Chapter 4, a spatial-orthogonal ASK transmitter architecture for high-speed terahertz wireless communication is presented. The self-sustaining oscillator-based transmitter architecture has an ultra-compact size and excellent power efficiency. With the proposed high-speed constant-load switch, significantly reduced modulation loss is achieved. Using polarization diversity and multi-level modulation, the throughput is largely enhanced. Array configuration is also adopted to enhance the link budget for higher signal quality and longer communication range. Fabricated in a 0.13-μm SiGe BiCMOS technology, the 220-GHz transmitter prototype achieves an EIRP of 21 dBm and dc-to-THz-radiation efficiency of 0.7% in each spatial channel. A 24.4-Gb/s total data rate over a 10-cm communication range is demonstrated. With an external Teflon lens system, the demonstrated communication range is further extended to 52 cm. Compared with prior art, this prototype demonstrates much higher transmitter efficiency.

In Chapter 5, an entirely-on-chip frequency-stabilization feedback mechanism is proposed, which avoids the use of both frequency dividers and off-chip references, achieving much lower system integration cost and power consumption. Using this mechanism, a 301.7-to-331.8-GHz source prototype is designed in a 0.13-μm SiGe BiCMOS technology. According to the measurement, the source consumes a dc power of only 51.7 mW. The output phase noise is -71.1 and -75.2 dBc/Hz at 100 kHz and 1 MHz offset, respectively. A -13.9-dBm probed output power is also achieved. Overall, the prototype source demonstrates the largest output frequency range and lowest power consumption while achieving comparable phase noise and output power performances with respect to the state of the art.

All the designs demonstrated in this thesis achieve good performances and

push the state of the art forward, paving the way for implementation of more sophisticated terahertz circuits and systems for future applications.

BIOGRAPHICAL SKETCH

Chen Jiang was born in Hubei, China. He received the B.Sc. and M.Sc. degree in Microelectronics from Fudan University, Shanghai, China, in 2010 and 2013, respectively, the M.Sc. degree in Electrical Engineering from Cornell University, Ithaca, NY, USA, in 2016.

From 2009 to 2013, Chen was a student research assistant in the Integrated Circuit Design (ICD) lab at Fudan University, Shanghai, China and worked on radio-frequency circuits and systems design. In 2013, he joined the Ultra-high-speed Nonlinear Integrated Circuits (UNIC) lab at Cornell University as a Ph.D. student, and his research topic is terahertz electronics for imaging, sensing and communication applications. From summer of 2016, he is also a visiting research assistant at University of Michigan, Ann Arbor. During summer of 2017, he worked in Qualcomm Inc. on research and implementation of low-cost high-performance radio-frequency digital-to-analog converters (RF-DACs).

He is currently a student member of the IEEE, a member of the IEEE Solid-State Circuits Society (SSCS) and the IEEE Microwave Theory and Techniques Society (MTT-S). He is also a reviewer for the IEEE Transactions on Circuits and Systems II: Express Briefs, the IEEE Microwave and Wireless Components Letters, the IET Electronics Letters, as well as the IEEE Communication Magazine. He was the recipient of the Irwin and Joan Jacobs Fellowship, Cornell University, in 2013, the Sporck Analog Design Fellowship, Cornell University, in 2014, the IEEE Solid-State Circuits Society Predoctoral Achievement Award in 2016 and the IEEE Microwave Theory and Techniques Society Graduate Fellowship Award in 2017.

This thesis is dedicated to my family.

ACKNOWLEDGEMENTS

Looking back into these years, a list of people who have helped me in one way or another is almost endless. To begin with, my sincerest gratitude goes to my advisor, Prof. Ehsan Afshari. To me, he is a perfect advisor and a great friend. He is knowledgeable, kind, energetic and humorous. He provides me with constant guidance, support and inspiration during my endeavor for cutting-edge research. He also gives me great freedom to work on the topics which interest me most, this allows me to fully explore my potential and keeps me passionate. I feel really lucky to join Cornell and have Ehsan as my advisor. Because of him, my Ph.D. life is fruitful and enjoyable.

I also would like to thank my committee members, Prof. Alyosha Molnar and Prof. Clifford Pollock, for their kind support and valuable advice on my research. During my graduate study, I have also received great support from other people in different organizations, such as Prof. Edwin Kan, Prof. Alyssa Apsel and Prof. Farhan Rana from Cornell University, Prof. Zhengya Zhang from the University of Michigan, Prof. Hua Wang from Georgia Institute of Technology as well as Dr. Andreia Cathelin from STMicroelectronics.

Special thanks to Ruonan Han, who was a member of our group and currently a faculty in Massachusetts Institute of Technology. When I first joined the group and knew nothing about terahertz design, he offered me plenty of help. Working with him was a great experience, which benefited me a lot. My appreciation also goes to other colleagues and great friends, the discussions with them are inspiring and valuable. They are Muhammad Adnan, Vahnood Pourahmad, Hamidreza Aghasi, Hamid Khatibi, Somayyeh Khiabani, Ali Mostajeran, Amirahmad Tarkeshdouz, Amirmasoud Ohadi, Saghar Seyedabbaszadeh, Hossein Naghavi, Najme Ebrahimiseraji, Farzad Khoeini, Samir Nooshabadi, Hyungjoo

Seo and Zainulabideen Khalifa. I would also like to thank Haining Wang, Yunfei Ma, and Visarute Pinrod for their help in my experiments.

In the summer of 2017, I had the chance to work with several great engineers on interesting projects at Qualcomm. Communicating with them helped me a lot. I want to thank Shahin Mehdizad Taleie, Dongwon Seo, Ashok Swaminathan, Bhushan Asuri, Nitz Saputra, Behnam Sedighi, Ibrahim Chamas and Joe Lai.

I would like to thank my girlfriend, Geyi Zheng. We have been through a lot of journeys together. Till now, we have lived in more than five cities in the United States already. Our life is everywhere, but you are always by my side. Thank you for being there for me, you are always my love and best friend.

At last, I would like to express my deepest gratitude to my mother, Xinhua Wang, and farther, Minghai Jiang. Throughout my journey of life, their constant support, understanding and love have helped me overcome all kinds of difficulties. I am the only child in the family, but they never complained about my constant absence. Instead, they support me with every decision I made and proud of me for every success I got. All the achievement I accomplished is because I have a warm family behind me.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

1.1 Overview of the Terahertz Spectrum

The terahertz (THz) band sits between the infrared and microwave bands in the electromagnetic spectrum, as shown in Fig. 1.1. The band of frequencies designated by the International Telecommunication Union (ITU) is from 0.3 to 3 THz (1 THz = 10^{12} Hz). A wider range from 0.1 to 10 THz is also often used in research works. Due to the wavelength range is from 0.1 to 1 mm, it is also often referred as submillimeter-wave band.

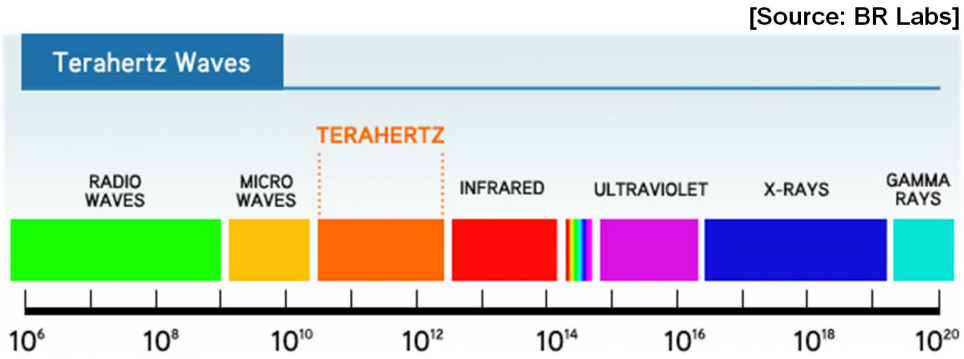


Figure 1.1: The terahertz band on the electromagnetic spectrum.

The unique characteristics of THz band promises many interesting applications. However, due to the fundamental limitation called "terahertz gap" [9], this frequency band still remains one of the least tapped regions on the electromagnetic spectrum, and the related applications are still in their infancies.

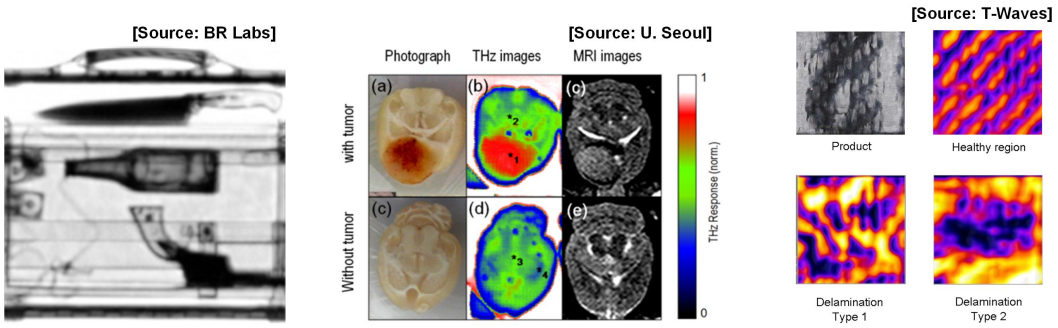
1.2 The Terahertz Applications

There are some unique applications possible for THz waves. Among them, imaging, spectroscopy and communication are mostly mentioned in researches.

1.2.1 Terahertz Imaging

Imaging is probably the most investigated application using the THz waves. Same as infrared and microwave radiation, THz radiation travels in a line of sight and is non-ionizing. It can penetrate a wide variaty of non-metal materials, such as cloth, paper, wood, plastic and ceramics, which makes it of interest for imaging. Thanks to the small wavelength, it can provide good lateral resolution, while the non-ionizing nature and low photon energy in general do not damage tissues and DNA, showing great advantage over X-rays.

Terahertz imaging has the potential to be used in a variety of areas. As shown in Fig. 1.2(a), THz imaging can be employed for security screening to detect concealed weapons and explosives [10]. The non-ionizing nature also attracts lots of research efforts on utilizing THz imaging for medical applications [11, 12]. Fig 1.2(b) shows an example experiment of using THz radiation to detect tumor tissues in a rat's brain. The application range can be extended to dentistry, dermatology and neurology as well. THz imaging has also shown its potential value in other fields, such as industrial production [Fig. 1.2(c)], material characterize [13], biology research [14] and many more.



(a) (b) (c)

Figure 1.2: Terahertz imaging has the potential to be used in a variety of areas: (a) security screening, (b) biomedical diagnosis and (c) industrial quality control.

1.2.2 Terahertz Spectroscopy

Spectroscopy is another important THz application. Prior research has shown that many types of molecules exhibit resonance absorption within the THz frequency range, and the associated absorption spectrum could be used as the "fingerprint" for material identifications [15]. Moreover, a lot of information about molecular structure and molecular motion can also be obtained from the spec-

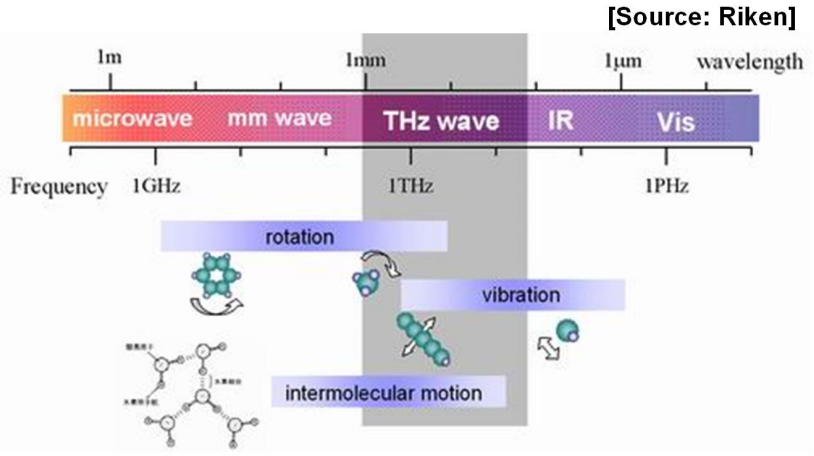


Figure 1.3: Many types of molecules exhibit resonance in the terahertz frequency range.

tra in this region, such as rotational spectra of light molecules, lower vibrational spectra of carbon chaines, the internal rotational motion of molecules and intermolecular vibrations [16].

THz spectroscopy technique can be used for indoor air quality monitoring, detection of toxic gas leaks, as well as breath analyses for monitoring health conditions [17]. Other applicable areas include material science [18], pharmacy [19] and astronomy [20].

1.2.3 Terahertz Communication

The demand for wireless communication throughput is expanding drastically, however, the spectrum resources are becoming more and more limited in conventional radio frequency (RF) bands. On the other hand, vast unallocated spectrum exists in THz range, which can provide ultra-wide bandwidth for high-speed communication. Compared with the broadcasting of conventional RF

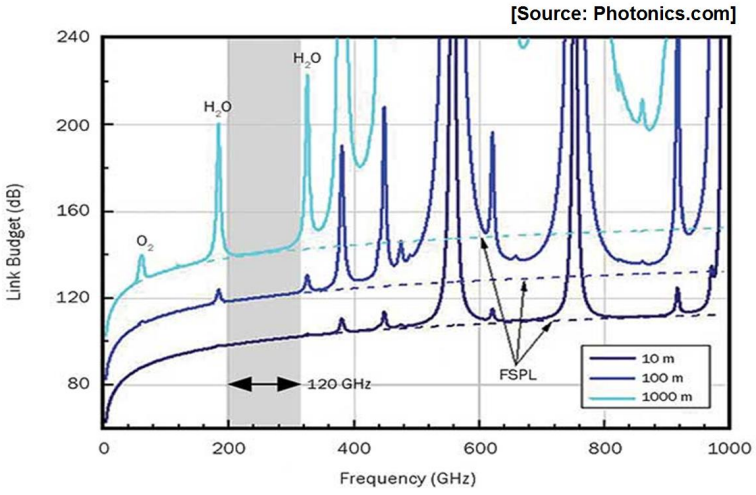


Figure 1.4: Path loss for terahertz wireless links.

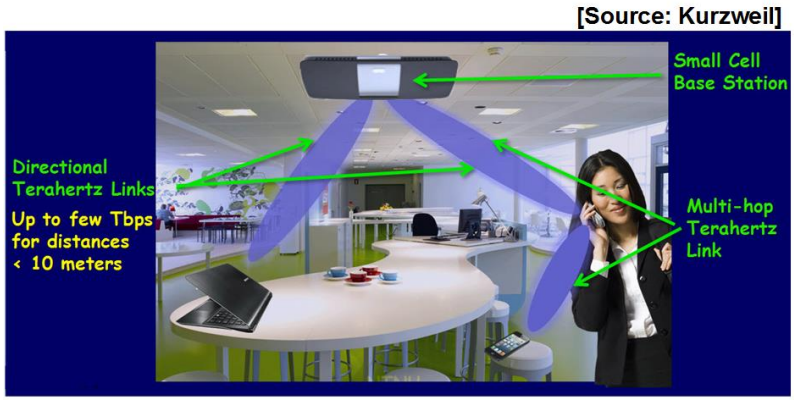


Figure 1.5: Indoor high speed connection using terahertz.

frequencies, the line-of-sight nature also provides better security.

Fig. 1.4 shows the path loss for wireless signals at different frequencies with a distance of 10 m, 100 m and 1000 m. The first low absorption window is from 200 GHz to 325 GHz, which provides more than 120 GHz usable bandwidth. There are already many research efforts on utilizing this bandwidth to realize high speed links for chip-to-chip, device-to-device and also indoor high speed interconnects [7, 21]. For the indoor wireless connection, due to the large path loss and possible interruption caused by interfering objects, steerable high-gain antennas are often required to connect from an reflected path in case the primary line-of-sight path is blocked.

Beside free space propagation, communication based on guided THz waves using THz fibers (such as bare metal waveguides, hollow-glass metallic waveguides and photonic crystal fibers) is also being investigated [21]. Compared to optical fibers, THz fibers can have a much simpler and cheaper integration and packaging since the CMOS-incompatible electro-optical conversions are avoided [22].

1.3 Why Silicon?

Unfortunately, to utilize this frequency range, many challenges exist, normally referred as the "terahertz gap". Researchers are approaching the "terahertz gap" from two sides: classical electronics from the lower side, as well as optics or photonics from the higher side. However, the THz range turns out to be too high for electronics but too low for optics or photonics, leaving it inefficient to deal with for both approaches. This also explains why it is the least explored spectrum.

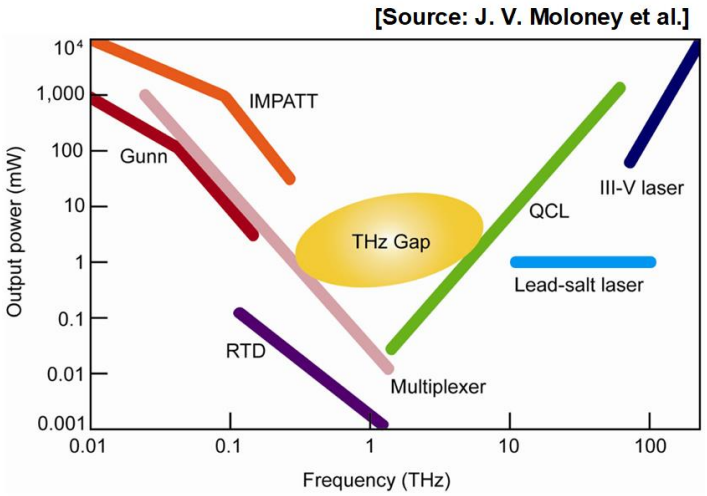


Figure 1.6: The terahertz gap.

Currently, THz systems are bulky and expensive. Sometimes, they require cryogenic condition (e.g. quantum cascade laser and bolometer) and are built with fragile structures (e.g. backward-wave vacuum tube), therefore low reliability and short lifetime are also critical issues for these systems [22]. Therefore, silicon platform (especially commercial low-cost CMOS and SiGe technologies) becomes very attractive. For the past few decades, silicon has shown its magi-

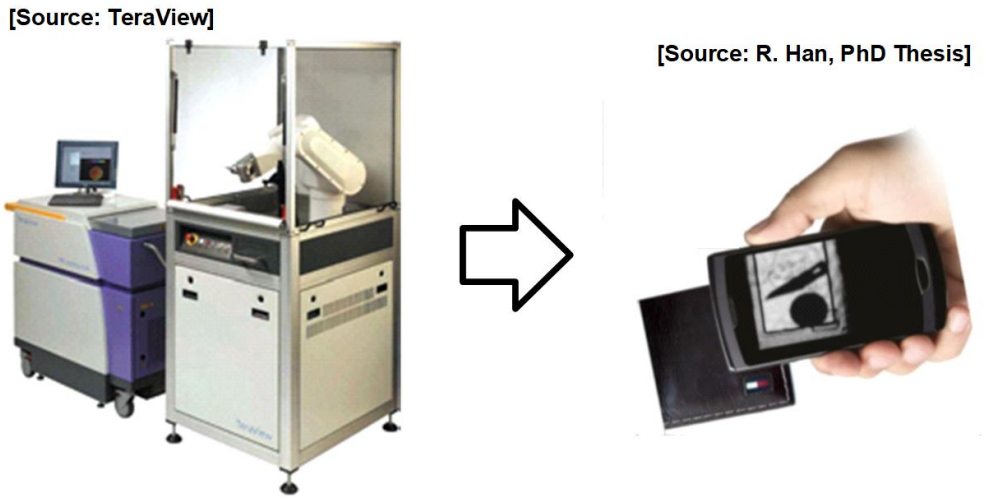


Figure 1.7: Current terahertz equipment and its conceptual silicon counterpart.

cal power of shrinking things, not only size but also price. If a THz system is integrated on silicon, one can expect significantly lower cost, smaller form factor, less power consumption, as well as room temperature operation. It is also easier to be integrated together with other SoCs for post signal processing to implement more sophisticated functionality. All these help to bring THz devices from advanced labs into our homes to improve our everyday lives.

1.4 Design Challenges of Silicon Terahertz Electronics

To implement a silicon THz system, major challenges reside in two aspects: signal generation and signal processing. Next, these challenges will be discussed in detail.

1.4.1 Challenges of Signal Generation

Generating the THz signal is the first step of implementing a THz system. In spite of the continuous advancement of the silicon fabrication technologies, the output power of THz signal can be generated on silicon is still limited, due to a couple of causes:

(i) Even though the feature size of the silicon device continues to shrink, the maximum frequency of oscillation, f_{max}, of the transistors (including the device interconnects) is still near 300 GHz. This sets a theoretical limitation, beyond which no fundamental oscillation nor power amplification is possible [23].

(ii) In advanced technology node, the thin gate oxide causes low breakdown voltage. This severely limits the fundamental and harmonic power generation, which are highly dependent on the voltage swing.

(iii) The passive structures fabricated on silicon normally have a limited quality factor, causing considerable amount of loss to signal propagation, resonance and radiation.

(iv) The inevitable electrical and magnetic coupling of the signal into the low-resistance silicon substrate adds additional loss.

Besides the limited absolute power, other challenges exist, such as limited dc-to-THz generation efficiency and signal source bandwidth. The former one is important for the battery life of future potable THz devices. The latter one has large impact on performances of many THz systems, such as spectroscopy and communication systems.

1.4.2 Challenges of Signal Processing

In applications like imaging and spectroscopy, signal processing mostly refers to signal detection or sensing. Due to the fact that signal frequency is higher than the device f_{max}, no pre-amplification is available to suppress device noise. Together with excessive passive loss, achieving high detection sensitivity is very challenging. More details about this will be discussed in Chapter 3.

In communication systems, beside signal detection, another important signal processing involved is the modulation. Beyond the device f_{max}, no power amplification is available, meaning the modulation path only adds loss to the generated or received THz signal. This causes very limited output power for the transmitter and limited sensitivity for the receiver. Overall, the result is small communication range and low SNR. More details about this will be discussed in Chapter 4.

1.5 Research Scope of This Thesis

To implement high-performance THz systems on silicon, the research scope of this thesis can be divided into the following parts:

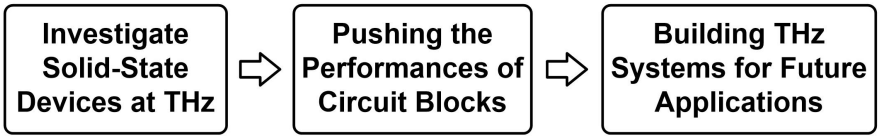


Figure 1.8: Research scope of this thesis.

(i) **Investigate solid-state devices at THz frequencies:** Unlike conventional

low-frequency design treating transistors either like current sources or switches inserted into a certain circuit topology, in this frequency band, efficacy of the transistors is very sensitive to their terminations. Consequently, it is beneficial to investigate the transistors by themselves and derive the optimal termination conditions for the desired performances. These would later be used as a guidance on designing of THz circuit blocks.

(ii) **Pushing the performance of circuit blocks:** Once the devices are chosen, the next step is to design passive surrounding networks that provide the devices with the optimal termination conditions. Due to the limited quality factor of the passive devices on chip, novel EM structures and circuit topologies need to be designed to push the circuit performances. In addition, harmonics are often used in THz circuits, this also creates room for "smart engineering" to utilize mode orthogonality of the harmonic waves to make the same EM structures have different desired behaviors at different harmonics.

(iii) **Building innovative THz systems for future applications:** Building systems in THz range is no longer just interconnecting circuit blocks. Due to the high frequency, floor plan and interconnection need to be carefully arranged. To optimize the system performance, oftentimes, the circuit blocks and system floor plan need to be co-designed from the very beginning. Although challenging, system architecture design has a large room for creativity.

In the following chapters, design a few state-of-the-art circuit prototypes will be demonstrated:

For signal generation, a wide-tuning efficient 210-GHz compact oscillator is designed using a device-centric methodology. The oscillator achieves a peak output power and dc-to-RF efficiency of 1.4 dBm and 2.4%, respectively. The frequency tuning range achieved is as wide as 10.6% [1].

For THz imaging application, a fully-integrated 320-GHz coherent imaging transmitter and receiver pair will be described [4, 5]. The transmitter chip achieves a peak radiated power of 2 mW and a peak EIRP of 21.1 dBm with a total dc power consumption of 605 mW. The receiver chip achieves an equivalent incoherent responsivity of more than 7.26 MV/W and a sensitivity of 70.1 pW under an integration bandwidth of 1 kHz. The total dc power consumption of the receiver chip is 117 mW. To our best knowledge, this is the first fully integrated coherent THz imaging transmitter and receiver pair demonstrated on silicon. This design also achieves around ten times better sensitivity compared with other state-of-the-art incoherent imagers.

For THz communication application, a high-speed efficient 220-GHz spatial-orthogonal ASK transmitter will be discussed [7]. It demonstrates a 24.4-Gb/s total data rate over a 10-cm communication range, as well as the highest transmitter efficiency among all recent published works.

Finally, this thesis also introduces a 301.7-to-331.8-GHz source with entirely-on-chip frequency-stabilization feedback loop [8], which eliminates the need for both frequency dividers and off-chip crystal oscillators, achieving much lower system integration cost and power consumption. The source achieves a power consumption as low as 51.7mW. The measured phase noise is -71.1 and -75.2dBc/Hz at 100kHz and 1MHz offset, respectively. A -13.9dBm probed output power is also achieved.

All the works mentioned above have achieved impressive performances, and shown the promising future for silicon THz electronics.

CHAPTER 2

EFFICIENT TERAHERTZ FREQUENCY GENERATION ON SILICON: A DEVICE-CENTRIC DESIGN METHODOLOGY

The first step of building any terahertz system is to generate the terahertz signals. In this chapter, we first focus on efficient terahertz signal generation circuits and the suitable design methodology to achieve the best performance.

2.1 Introduction on Terahertz Frequency Generation

It has been shown in Chapter 1 that, the terahertz bands are gaining increasing attentions these days for the potential applications in imaging [5], sensing [10], spectroscopy [17] and communication [21]. These applications can be used in a wide range of areas, such as military, security, biomedical analysis, material science, astronomy and so on [10]–[21]. However, all these applications desire low-cost and effective signal sources, which currently are still challenging due to the "terahertz gap" [9], which is also discussed in Chapter 1.

From a system point of view, several performances are desired from a signal source:

(i) **High output power:** This is required to achieve a good signal to noise ratio. It is a natural desire for almost all applications.

(ii) **Wide tuning range to achieve larger signal bandwidth:** In communication systems, higher bandwidth helps to achieve better throughput. In spectroscopy, it means larger spectrum coverage.

(iii) **Good power efficiency and small physical size:** This is desired for en-

hancing the battery life and lowering the cost of future potable terahertz devices.

(iv) **Low phase noise:** It is normally needed in coherent systems for better signal quality.

To generate signal in this band, there are two typical approaches: harmonic oscillators and multiplier chains [29]. Both of them rely on the nonlinearity of devices, but the harmonic oscillators do not need RF driving inputs and generally are more power efficient and occupy smaller area [29]. These features make them more suitable for system integration. As a result, this thesis focus more on oscillator based signal sources.

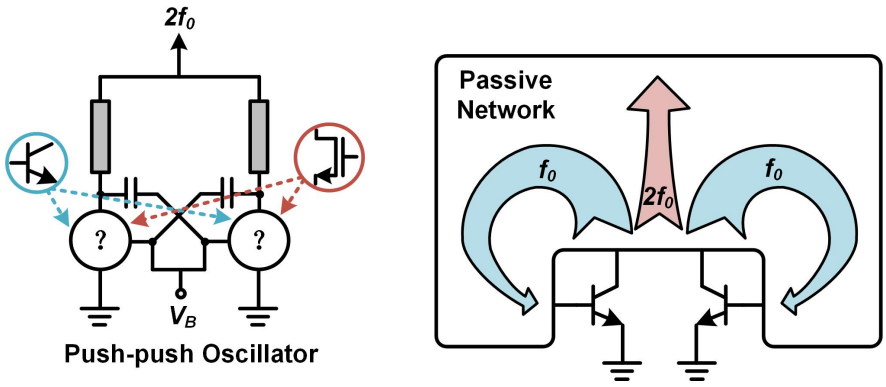
Recently, many research efforts have been paid to silicon THz oscillators and significant progress has been made. Reported in [30], fabricated with a 65-nm CMOS technology, the 482-GHz triple-push oscillator achieves -7.9-dBm probed output power. In [31], the 16-element 280-GHz distributed active radiator (DAR) on a 45-nm SOI CMOS technology achieves a radiated power of -7.2 dBm and an EIRP of 9.4 dBm. In [32], on a 65-nm CMOS technology, 390 μW of power is radiated from the 288-GHz triple-push oscillator with 0.14% efficiency. In [33], a probed power of 2.6 mW and efficiency of 1.14% is demonstrated with 8 coupled oscillators on 65-nm CMOS. In [3], fabricated with a 0.13-μm SiGe BiCMOS technology, the phase-locked source can radiate 3.3 mW power with 0.54% peak dc-to-radiation efficiency. Normally, THz harmonic oscillators have small frequency tuning ranges. To alleviate this drawback, new techniques have been introduced. In [34], a novel frequency tuning mechanism based on coupled oscillators is explained and 4.5% tuning range is achieved with a 290-GHz prototype without any varactor. In [35], a 3.5% tuning range is achieved by a

200-GHz inductively-tuned VCO. In [36], with an additional mode switching scheme, the 190.5-GHz VCO can provide a total tuning range of 20.7%.

In the rest of this chapter, a device-centric bottom-up design methodology will be introduced. With this new design methodology, an efficient 210-GHz compact harmonic oscillator prototype is designed with a 0.13-μm SiGe BiCMOS technology.

2.2 Overview of the Oscillator Design Flow

Typically, in an oscillator design, two methods can be used. Shown in Fig. 2.1(a) is the topology-based top-down design method, which is often used in low frequency oscillators design. In this design method, the first step is to choose a proper oscillator topology, and then transistors are inserted into the topology. However, in THz harmonic oscillators, the fundamental oscillation frequency is normally very close the device f_{max} , which means the transistors are working



(a) (b)

Figure 2.1: Oscillator design methodologies: (a) topology-based top-down method and (b) device-centric bottom-up method.

near their activity boundary and their efficacy is very sensitive to their termination conditions. Under this circumstance, blindly inserting the transistors into a certain topology is not effective. To achieve better overall performances, a device-centric bottom-up design method is used, as shown Fig. 2.1(b). In this method, the transistors are first investigated under the desired working frequency and a suitable surrounding passive network is designed to provide the needed termination conditions for the transistors for optimal harmonic power generation and extraction.

2.2.1 Active Devices Investigation

The first step is to choose a suitable device size. Larger size of a transistor can handle higher current, hence more power. However, the longer interconnect causes more loss to lower the device f_{max} . Also, larger parasitic capacitances will make high frequency oscillation more difficult. As a trade-off, bipolar transistors with two emitters ($n_{be} = 2$) and each has emitter length and width $L_E/W_E = 4\ \mu m/0.27\ \mu m$ is chosen in the oscillator design.

The harmonic generation inside the oscillators is based on the nonlinearity of the transistors, which goes stronger with larger fundamental voltage swing. Due to the linearity of the passive network (including load), larger voltage swing means higher passive loss, and larger fundamental power coming out of the transistors is needed to sustain the oscillation. Therefore, first of all, we seek for the conditions that maximize the oscillator fundamental power.

As shown in Fig. 2.2, to maximize the output power at the collector of the transistor, phase of the collector voltage v_c needs to be aligned with the collector

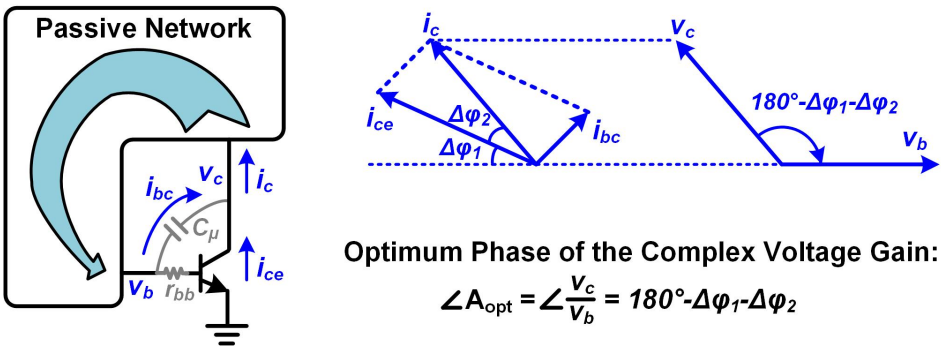


Figure 2.2: Extra phase shift needed for maximum fundamental oscillation caused by the intrinsic base delay and the feed-forward effect in a bipolar transistor.

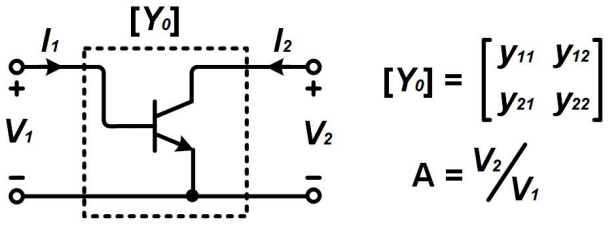


Figure 2.3: Two-port network representation of an npn transistor.

current i_c. Due to the intrinsic base delay caused by the parasitic base resistance r_{bb} and feed-forward effect caused by the parasitic base-collector capacitance C_μ, the optimum phase shift from v_c to v_b is $180° - \Delta\phi_1 - \Delta\phi_2$ instead of the conventional 180° inversion [37].

This could also be proved with a more formal way. As shown in Fig. 2.3, the npn transistor is modeled as a two-port network with large-signal Y-parameters:

$$[Y_0] = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}. \tag{2.1}$$

Values of the parameters can be obtained with simulation or measurement. Since the total power coming out of the transistor (P_{out}) is expressed as:

$$P_{out} = -Re(V_1 I_1^*) - Re(V_2 I_2^*) \tag{2.2}$$

in which, (V_1, I_1) and (V_2, I_2) are the rms voltage and current of the base and collector node. Using the Y-parameters, the current can be expressed as:

$$I_1 = y_{11}V_1 + y_{12}V_2 \tag{2.3}$$

$$I_2 = y_{21}V_1 + y_{22}V_2 \ . \tag{2.4}$$

If we define a base-to-collector complex voltage gain as:

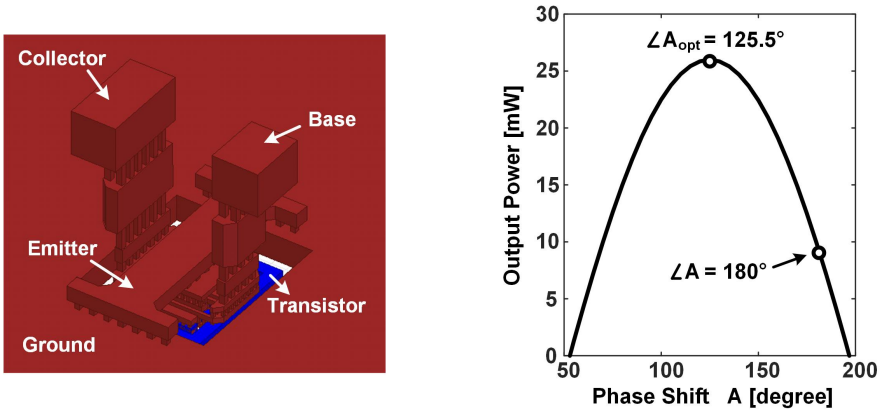
$$A = \frac{V_2}{V_1} \ , \tag{2.5}$$

with equation (2.3) and (2.4), equation (2.2) can be rewritten as:

$$P_{out} = -g_{11}|V_1|^2 - g_{22}|V_2|^2 - |V_1||V_2|[(g_{12} + g_{21})\cos\angle A + (b_{21} - b_{12})\sin\angle A] \ , \tag{2.6}$$

in which, g_{ij} and b_{ij} are the real and imaginary parts of y_{ij}, respectively. To maximize the third term of equation (2.6), the optimum phase $\angle A_{opt}$ is [30, 37]:

$$\angle A_{opt} = -(y_{21} + y_{12}^*) \ . \tag{2.7}$$



(a) (b)

Figure 2.4: The transistor with $n_{be} = 2$, $L_E/W_E = 4\mu m/0.27\mu m$ and biased at $V_c = 1.8\ V$, $V_b = 0.88\ V$: (a) 3-D interconnect model and (b) simulated output fundamental power with different phase shift between v_c and v_b at 110 GHz.

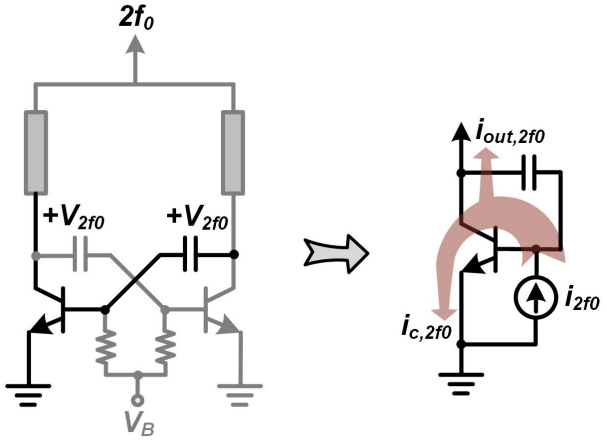


Figure 2.5: Self-power-cancellation effect in conventional push-push harmonic oscillators.

When frequency increases, the optimum phase condition deviates further away from the conventional 180°. With the interconnect shown in Fig. 2.4(a) and bias of $V_c = 1.8\ V$ and $V_b = 0.88\ V$, the simulated output fundamental power of the transistor at 110 GHz with different phase shift between v_c and v_b is given in Fig. 2.4(b), which shows a optimum collector-to-base phase shift of 125.5°. As a result, the passive network needs to be able to provide this optimum phase shift in order to maximize fundamental oscillation swing.

However, this is not the only requirement for the passive network. Shown in Fig. 2.5 is a simplified conventional push-push harmonic oscillator and its equivalent half-circuit under the second harmonic. Since for the second harmonic signals, two sides of the circuit appears to be in phase, an equivalent diode connection forms between the transistor base and collector. Due to this equivalent diode connection, the generated second harmonic current sees a small impedance across the transistor, therefore, a large part of the current flows back into the ground. This is called the self-power loading/cancellation effect [37]. To get rid of this effect, the passive network in Fig. 2.1(b) should be able

to isolate the transistor base and collector at the second harmonic frequency in order to cut out this unwanted current flow path. Also, in Fig. 2.5, for separate dc biasing of the transistors, capacitors are used between base and collector nodes. However, at high frequency, capacitors normally have limited quality factor and large parasitics, which will degrade the performance of the oscillator. As a result, it is also desired that the passive network can naturally provide dc separation of the transistor base and collector.

2.2.2 Passive Network Design

According to the previous investigation of the transistors, to achieve optimal harmonic power generation, the passive network surrounding the transistors needs to be able to simultaneously provide an optimal collector-to-base voltage phase shift, base-collector isolation at the second harmonic frequency as well as base-collector dc separation. Next, details of how these requirements are met will be discussed.

To provide an optimal collector-to-base phase shift, the passive network can include a self-feeding transmission line between the transistor base and collector, forming a self-feeding oscillator structure [37]. First, as shown in Fig. 2.6(a), two of the self-feeding oscillators are placed next to each other. They are two separate systems with very weak electric fields between them. In principle, they can oscillate in-phase, out-of-phase, or any combination of the two to form an arbitrary phase relation. Here, we first assume they are out-of-phase, the reason will be discussed later. Next, as shown in Fig. 2.6(b), the two oscillators are moved closer with a small section of the self-feeding lines touching each

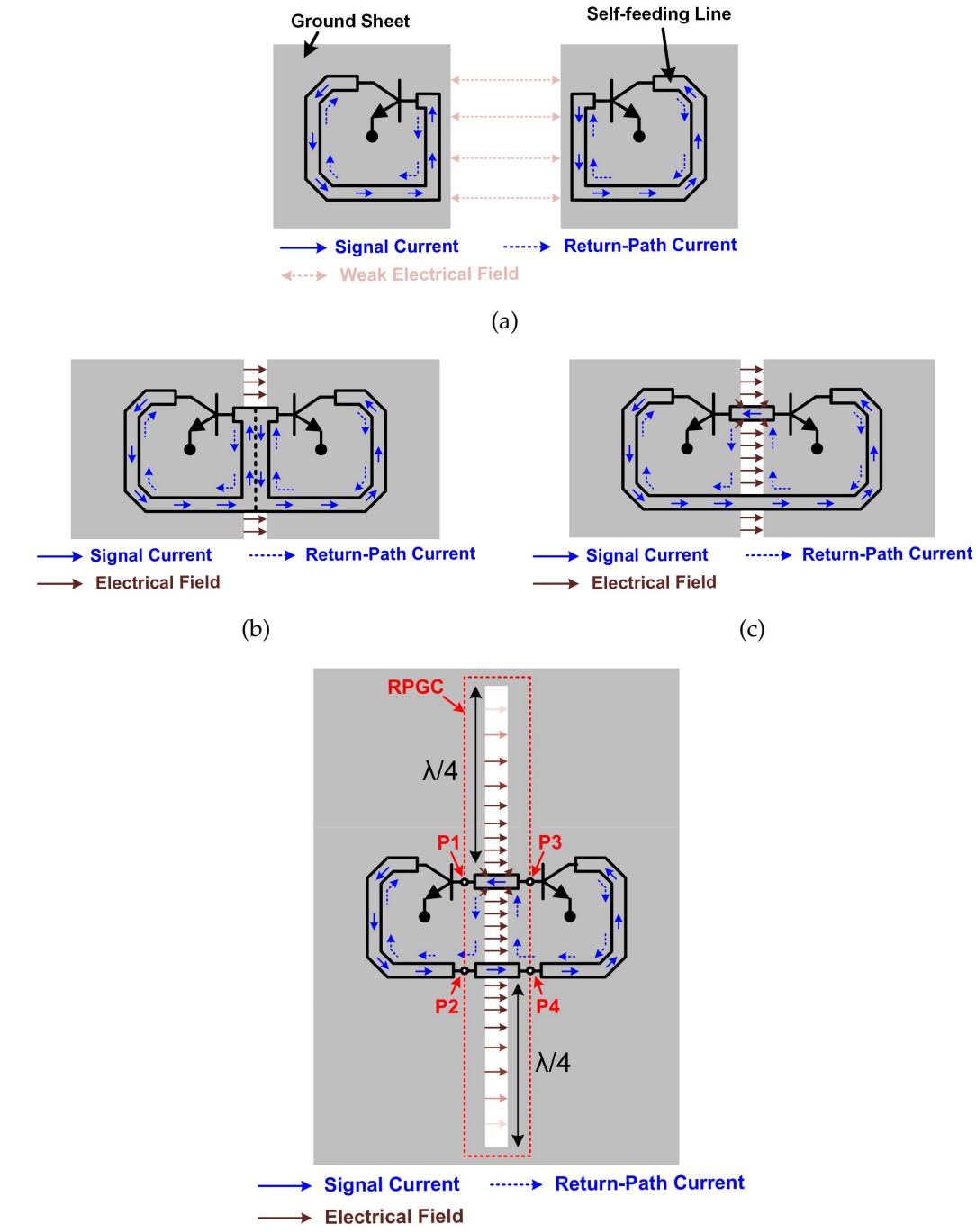


Figure 2.6: Evolving of the return-path gap coupler: (a) two self-feeding oscillators placed apart, (b) two self-feeding oscillators with self-feeding lines touching each other, (c) touched section removed and (d) quarter-wave slots placed on top and bottom. Figures not drawn to scale.

other and forcing a relative potential between them. Please note that length of the touched section drawn in Fig. 2.6(b) is exaggerated. After the touching, the inner edges of the ground sheets now have different potentials and electrical fields build up. Inside the touched section, the current is exactly out-of-phase and will cancel each other, which means this section can be removed. As a result, a gap structure shown in Fig. 2.6(c) is formed. There is one issue with this structure that, the inner edges of the ground sheets still have different potentials. To deal with this issue, as shown in Fig. 2.6(d), two quarter-wave slots are placed both on top and bottom of the structure to separate the local grounds from the global ground to allow the different potentials. However, as in Fig. 2.6(d), standing waves are formed inside both the upper and lower slots and they are in phase, which means this structure will radiate the fundamental power and cause additional loss to the oscillator. To get rid of this undesired radiation, both slots are split into two slot lines and bent to the horizontal direction, as shown in Fig. 2.7, so that the standing waves inside the left and right slot lines are out-of-phase, which means they will cancel each other in the far field and no radiation is formed. The slot lines are also folded in order to minimize the physical size. Finally, the return-path gap coupler (RPGC) structure is formed. Under the assumed odd mode, transmission between $P_1(P_3)$ to $P_2(P_4)$ is supported by the return-path current on the edges of the gap, as shown in Fig. 2.7. However, under even mode, no return-path current can be induced and the gap looks like a CPW transmission line without signal trace in the middle, so the transmission is blocked. To verify this, the RPGC is then simulated under both odd-mode and even-mode excitation as shown in Fig. 2.8(a) and Fig. 2.8(b), respectively. The results are shown in Fig. 2.8(c). As we can see, under the odd-mode excitation, the RPGC is almost transparent within a large

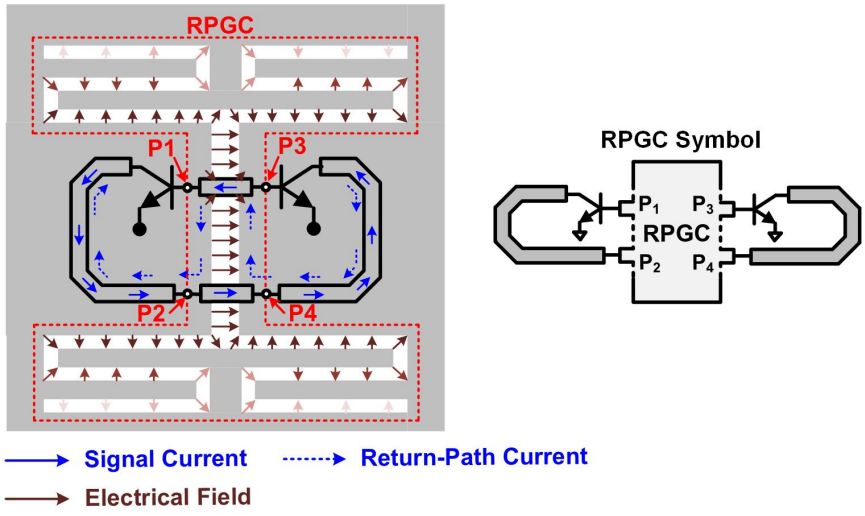


Figure 2.7: The surrounding passive network structure and the symbol representation.

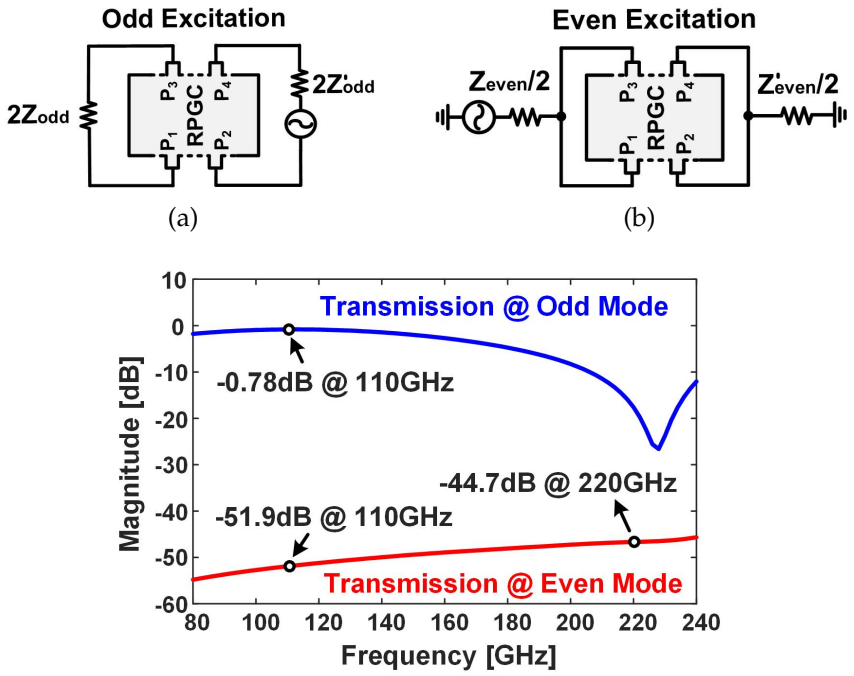


Figure 2.8: The return-path gap coupler under (a) odd-mode and (b) even-mode excitation as well as (c) the simulated transmission between $P_1(P_3)$ to $P_2(P_4)$.

bandwidth around 110 GHz, which is very helpful to achieve wide frequency tuning range with reasonable output power fluctuation for the oscillator. At 110 GHz, the insertion loss of this RPGC is simulated to be as low as 0.78 dB. At frequencies much higher than 110 GHz, the slot lines at the top and bottom of the RPGC are no longer near quarter-wave length and operation of the gap is disturbed, so significantly higher loss is observed. Under the even-mode excitation, the RPGC is opaque with more than 40 dB isolation through out the whole simulated frequency band, as shown in Fig. 2.8(c). In fact, if we take the gap as a two-metal waveguide structure, balanced wave can propagate in TM mode. However, with this geometry, the cut-off frequency of the lowest TM mode is around 6 THz [37], which means, within the frequency range of concern, the RPGC is always opaque to even-mode signals.

Previously, we assumed the two oscillators in Fig. 2.6(a) are out-of-phase, but by symmetry, they are possible to be in-phase with the surrounding passive network shown in Fig. 2.7. However, if they are in-phase, the RPGC will work under the even-mode excitation with signals symmetrically applied to the ports. Under this case, the RPGC will be opaque and the feedback between the base and collector nodes of the transistors are cut out, which means no oscillation is possible to exist. Consequently, the two oscillators can only oscillate out-of-phase and the assumption is valid. At the same time, the generated second harmonic signals appear to be in-phase on the two sides of the RPGC, and for the same reason, base-collector isolation at the second harmonic is achieved. Besides, the RPGC structure also naturally separates the dc of transistors collector and base. Therefore, with the self-feeding lines providing the optimum collector-to-base phase shift and the RPGC supporting base-collector isolation at the second harmonic as well as DC, all the requirements are achieved with

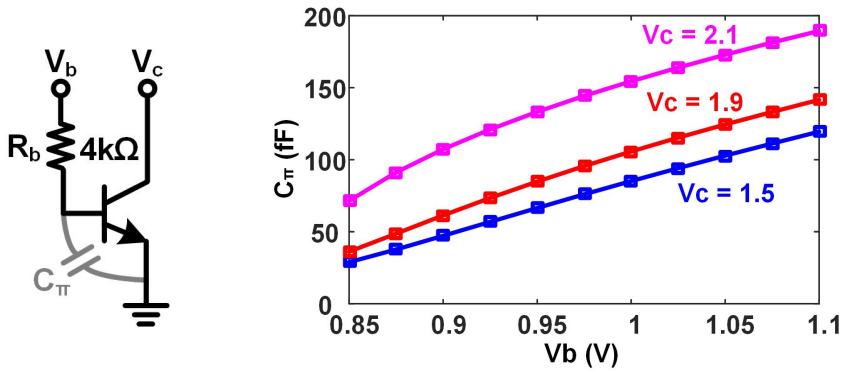
this passive network shown in Fig. 2.7 for optimal harmonic power generation.

2.2.3 Parasitic Frequency Tuning Mechanism

Besides achieving optimal output harmonic power and efficiency, wide tuning range is also highly desired. The most widely used frequency tuning mechanism is the varactor-based tuning. However, at this frequency, varactors exhibit low C_{max}/C_{min} and high loss due to large parasitics and poor quality factor. As a result, they can only provide very limited frequency tuning range while hurting the output power and phase noise of the oscillator. Inductive tuning is another alternative, however, it contributes high loss and also occupies large area [35]. Mode-switching technique can be used together with either varactor-based or inductive tuning to obtain larger tuning range [36], but still at the expense of sacrificing output power, efficiency, complexity and area. In this work, parasitic tuning scheme is used to achieve wide tuning range without hurting other performances of the oscillator.

It is known that the parasitic capacitances of a bipolar transistor are very sensitive to the bias points. For the transistor used in this design, biased through a 4-kΩ resistor at the base as shown in Fig. 2.9(a), the simulated base-emitter parasitic capacitance C_π under different base bias V_b and collector bias V_c is shown in Fig. 2.9(b). It shows that C_π can be changed by a large range with manipulating the bias, which means a wide frequency tuning is achievable with parasitic tuning mechanism without using any lossy varactor or tunable inductor, and as a result, good output power and phase noise performances can be maintained.

With changing of biasing, parasitics of the transistor are changed by a large



(a) (b)

Figure 2.9: Simulation of the base-emitter parasitic capacitance C_π of the bipolar transistor ($n_{be} = 2$, $L_E/W_E = 4\mu m/0.27\mu m$): (a) schematic and (b) results.

range. This can provide the capability of frequency tuning, but will also alter the optimum collector-to-base phase condition of the transistors, since the phase shift caused by the intrinsic base delay and feed-forward effect ($\Delta\phi_1$ and $\Delta\phi_2$ shown in Fig. 2.2) also depends on the parasitics. To evaluate this impact, with collector bias V_c fixed at 1.8 V, the optimum phase condition of the transistors as well as the fundamental oscillation frequency at different base bias points V_b are simulated. The results are shown in Fig. 2.10. It can be seen that, the optimum phase condition of the transistors varies by a large range with changing of bias. Then, phase shift provided by the surrounding passive network at different frequencies is also simulated and plotted in Fig. 2.10. With careful design, the change of the phase shift provided by the passive network follows a similar trend with the optimum phase condition of the transistors. This is possible because when V_b becomes higher, the larger parasitic capacitances of the transistors cause a longer intrinsic base delay and larger feed-forward effect, or a larger $\Delta\phi_1 + \Delta\phi_2$ in Fig. 2.2, which leads to a smaller optimum phase condition between v_c and v_b. At the same time, the larger parasitic capacitances of the

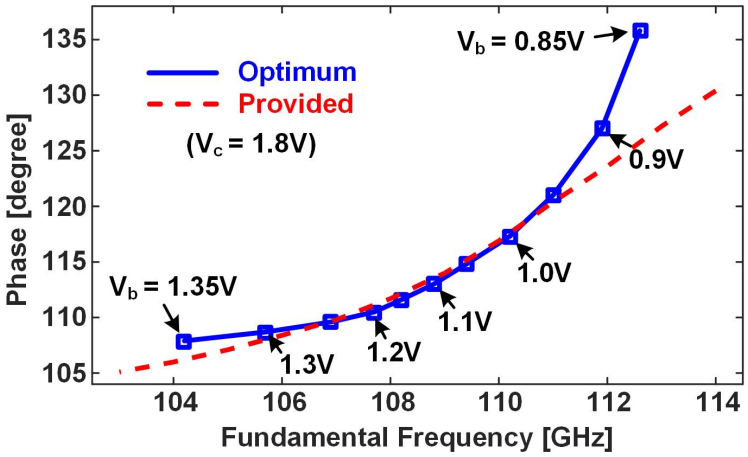


Figure 2.10: Simulated optimum phase condition of the transistors and phase shift provided by the passive network under different frequencies. Collector bias V_c is fixed at 1.8 V.

transistors cause a lower oscillation frequency, and consequently, self-feeding lines with the same physical length will provide a smaller phase shift. Finally, according to the simulation results shown in Fig. 2.10, the surrounding passive network can provide a near-optimum phase shift inside almost the whole oscillator tuning range. In addition to this, as mentioned previously, the operation of the RPGC is not frequency dependent and the insertion loss of it under the odd mode is kept low within a wide bandwidth, as shown in Fig. 2.8(c). Consequently, with the parasitic tuning mechanism and the surrounding passive network shown in Fig. 2.7, a wide frequency tuning range is achieved and optimal terminations are provided to the transistors within almost the whole tuning range, which means large output power, high harmonic generation efficiency as well as wide frequency tuning range can be obtained simultaneously. Without relying on low-quality varactors, good phase noise performance can be also achieved.

2.3 Design Case: A Wide-Tuning Efficient 210-GHz Compact Oscillator

2.3.1 Circuit Design

The schematic of the proposed 210GHz compact harmonic oscillator is shown in Fig. 2.11. It is composed of two bipolar transistors ($n_{be} = 2$, $L_E/W_E = 4\mu m/0.27\mu m$), the optimized passive surrounding network described in Section 2.2.2 and the probing pad. The second harmonic power is extracted from the base nodes of the transistors for better harmonic generation efficiency [3]. Since the two sides of the oscillator is out-of-phase, node A in Fig. 2.11 presents virtual ground at the fundamental frequency. As a result, only the second harmonic signal will be sent to the pad. The base bias is applied at the feed line to the probing pad through a 4-kΩ resistor. The collector bias is applied at the

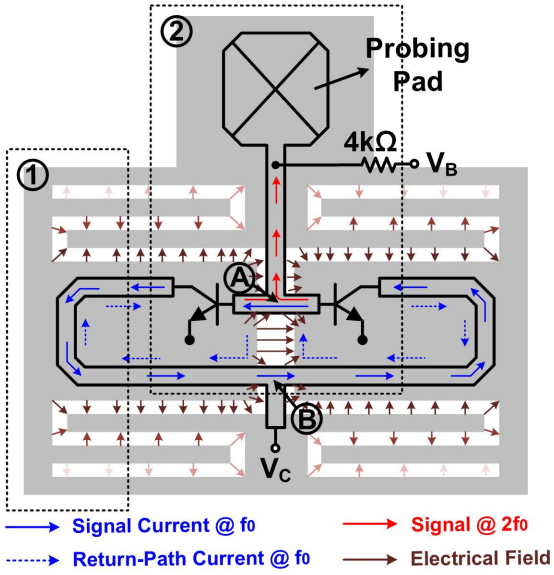


Figure 2.11: Schematic of the 210-GHz compact harmonic oscillator.

center of the self-feeding lines on the bottom, as shown in Fig. 2.11. For the same reason, node B in Fig. 2.11 also presents virtual ground at the fundamental frequency, so the parasitic capacitance and inductance introduced by the dc pad and bond wire for collector biasing V_c doesn't affect the fundamental oscillation. In addition, the second harmonic signal is blocked by the RPGC, and the generated harmonic power will directly flow to the pad without feeling much impact caused by this parasitics at node B. The 4-kΩ large resistor also isolates the parasitics of the dc pad and bond wire for base biasing V_b at both fundamental and harmonic frequencies. As a results, the chip is robust without relying on good on-chip decoupling of the dc biases.

Fig. 2.12(a) shows part of the 3-D structure of the slot lines and self-feeding line in the oscillator (area denoted with "1" in Fig. 2.11). Cross section of this 3-D structure is also given in Fig. 2.12(b). The self-feeding lines are realized using grounded CPW (G-CPW) lines. The signal trace is implemented with the 3-μm-thick top copper (M6), and an overlapped M1-to-M3 ground plane is placed underneath while M1-to-M6 stacked ground walls are placed on the two sides. As shown in Fig. 2.12(b), the width of the self-feeding lines are 6 μm and the distance to the ground plane and ground walls are 7.61 μm and 4 μm, respectively. According to the HFSS simulation, the characteristic impedance of the self-feeding lines is 49 Ω. The width of the slot lines is 4 μm, and the distance between two slots after folding is 5 μm, also shown in Fig. 2.12(b).

In order to efficiently deliver the generated oscillator harmonic power to the pad, it is desired to have a simple matching network and short feed line to the pad in order to minimize the loss. The 3-D view of the probing pad and the oscillator output matching is shown in Fig. 2.13, which is also the area denoted

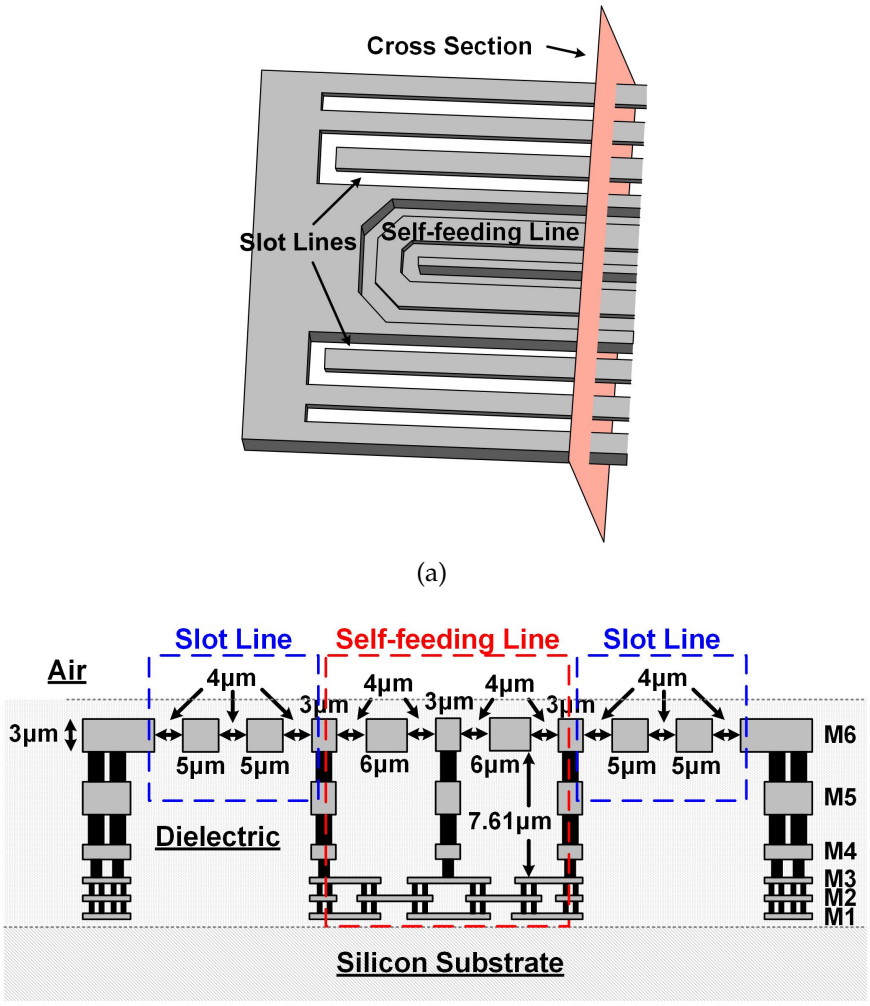


Figure 2.12: Structure of the slot lines and self-feeding lines: (a) 3-D view and (b) cross section.

as "2" in Fig. 2.11. In this design, the probing pad itself works as part of the matching network, and it is shaped to have a proper input impedance Z_A so that a simpler transmission line section is enough for the matching, as shown in Fig. 2.13. The pad is implemented on the 3-μm-thick top metal M6 with a 0.88-μm-thick aluminum layer on top. It is also shielded with the M1-to-M6 stacked ground walls and an overlapped M1-to-M2 ground plane. According to the simulation, the optimum load for the oscillator is 12 Ω, so a dimension

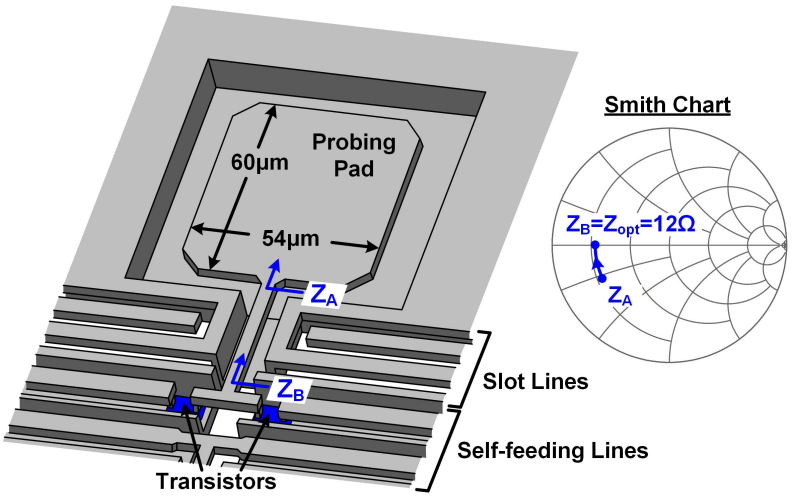


Figure 2.13: 3-D view of the custom-designed probing pad and output matching scheme on a smith chart.

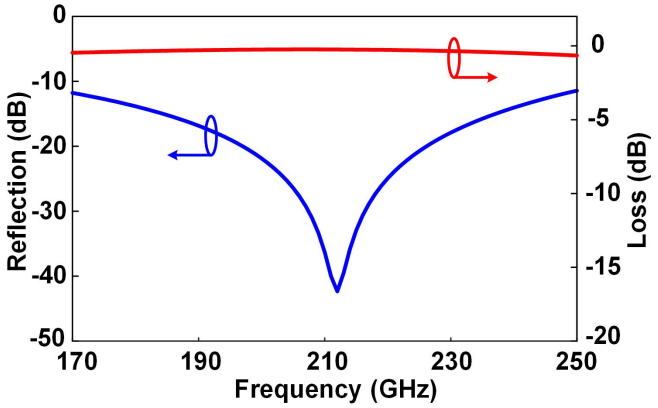


Figure 2.14: Simulated reflection and insertion loss of the output matching with frequencies.

of 60 μm by 54 μm is chosen for the probing pad to get an input impedance of $Z_A = (11.7 - j11.2)\Omega$ (assuming the 50-Ω probe load is connected to the center of the pad) that a small section of transmission line (23 μm long and 4 μm wide) could transform Z_A to the optimum 12-Ω load, as shown in the smith chart in Fig. 2.13. The simulated reflection coefficient as well as insertion loss of the whole output matching network including pad are shown in Fig. 2.14. This

output matching has a wide bandwidth and very low insertion loss. At center frequency 210 GHz, the simulated loss is as small as 0.24 dB.

2.3.2 Experimental Results

The compact 210-GHz harmonic oscillator prototype is implemented with the STMicroelectronics 0.13-μm SiGe:C BiCMOS process with a chip area of 290×275 μm^2 and a core area of only 290×95 μm^2. The microphotograph of the chip is shown in Fig. 2.15. The frequency and spectrum measurement setup is shown in Fig. 2.16(a). The output signal is probed with a Cascade i220 GSG waveguide probe. Using the VDI WR-5.1 even harmonic mixer (EHM), the probed signal is down-converted by mixing with the 16^{th} harmonic of a 13.58-GHz LO signal provided by the signal source. The down-converted signal is then observed on the spectrum analyzer. With the collector and base biases of 1.7 V and 0.86 V, respectively, the measured down-converted spectrum is shown in Fig. 2.17. The phase noise measurement result is shown in Fig. 2.18. At 1-MHz offset, it is

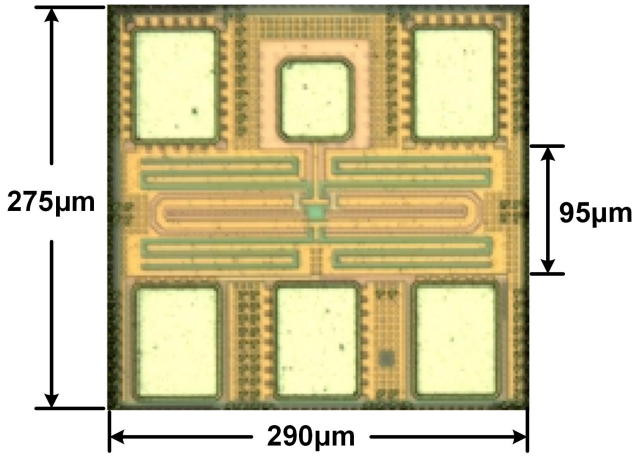


Figure 2.15: The microphotograph of the oscillator chip with core size of only 290×95 μm^2.

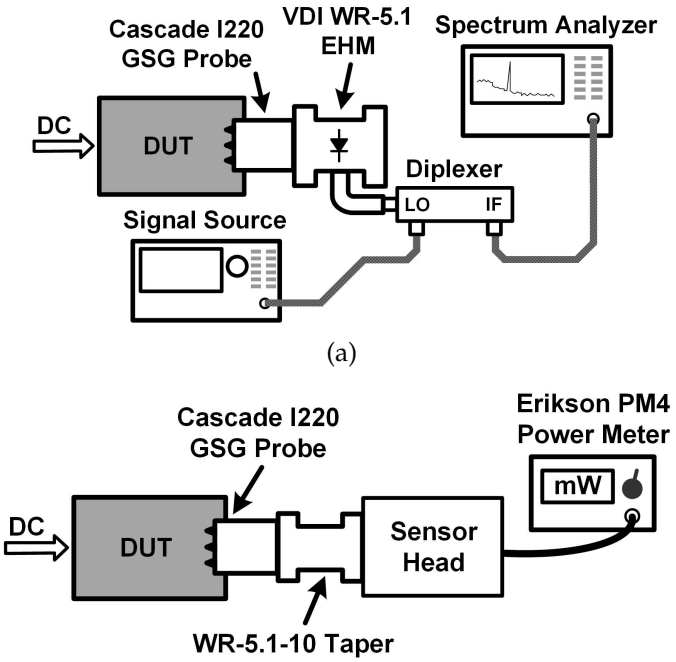


Figure 2.16: The measurement setups: (a) frequency/spectrum measurement and (b) power measurement.

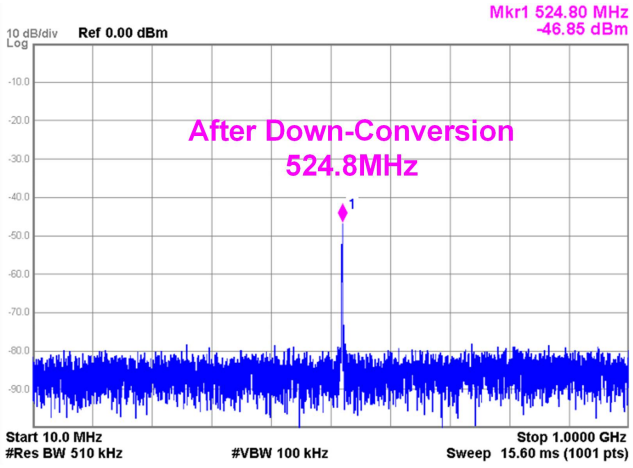


Figure 2.17: The measured output spectrum after down-conversion. With this 0.52 GHz IF frequency, the output frequency is calculated to be 217.8 GHz.

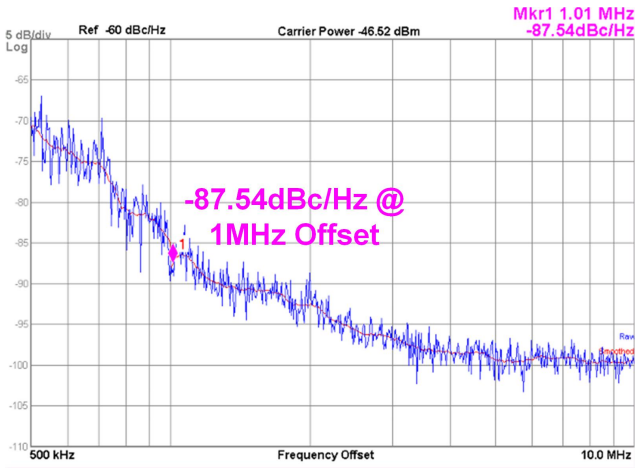
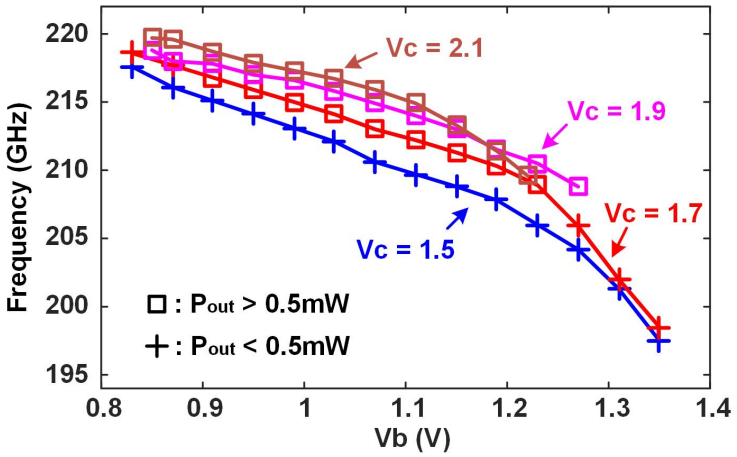
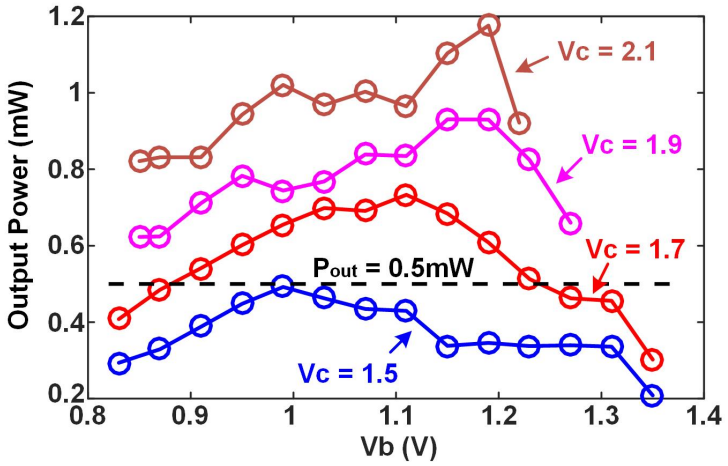


Figure 2.18: The measured phase noise of the oscillator. At 1MHz offset, it is -87.5 dBc/Hz.

measured to be -87.5 dBc/Hz. The power measurement setup is shown in Fig. 2.16(b), in which, the probed output signal power is measured by the Erickson PM4 power meter. Under different bias points, the measured output frequency and the corresponding output power are shown in Fig. 2.19. In the results shown in Fig. 2.19(b), the 5.2 dB probe loss and the 0.4 dB WR-5.1-to-10 taper waveguide loss are de-embedded. According to Fig. 2.19(a), the oscillator can be tuned from 197.5 GHz to 219.7 GHz, which is around 10.6% compared to the center frequency. In real applications, the tuning range that matters is the range inside which a certain amount of output power can be maintained. To better evaluate the tuning performance, a usable frequency range (UFR) is defined as the tuning range inside which the oscillator output power is always higher than 0.5 mW. Thanks to the fact that the passive network can provide near-optimum terminations for the transistors inside a large bandwidth as mentioned in Section 2.2.3, a wide UFR from 208.8 GHz to 219.7 GHz is achieved, which is around 5.2 % compared to the center frequency. To push the output power of the oscillator to its limit, the collector bias V_c is further increased. The measured



(a)



(b)

Figure 2.19: The measured (a) frequency tuning and (b) output power under different bias points.

peak output power and the corresponding dc-to-RF efficiencies under different collector bias V_c are shown in Fig. 2.20. The peak output power of the oscillator is about 1.37mW (or 1.4dBm) and the peak dc-to-RF efficiency is 2.4%.

In Table 2.1, the performances of the 210-GHz compact oscillator prototype is summarized and a comparison with other state-of-the-art silicon oscillators in this band is given. The oscillator achieves very high output power with ex-

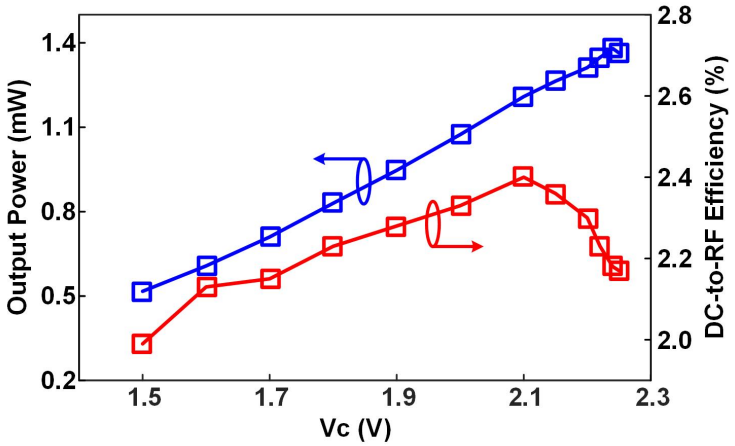


Figure 2.20: The measured peak output power and the corresponding dc-to-RF efficiencies under different collector bias V_c.

cellent dc-to-RF efficiency, as well as wide tuning range, low phase noise and very compact size.

A figure of merit generally used in comparing VCO designs in low frequencies is defined as below [38]:

$$FoM_T = L(\Delta f) - 20\lg(\frac{f_0}{\Delta f}\frac{TR}{10}) + 10\lg(\frac{P_{DC}}{1mW}) \tag{2.8}$$

in which, $L(\Delta f)$ is the phase noise of the oscillator at a frequency offset of Δf, f_0 is the output center frequency, TR is the frequency tuning range in percentage and P_{DC} is the total dc power consumption. However, FoM_T can not capture the oscillator output power performance, which is one of the key performances desired in this band. In [35], the FoM_T is revised as the following:

$$FoM_{TP} = L(\Delta f) - 20\lg(\frac{f_0}{\Delta f}\frac{TR}{10}) + 10\lg(\frac{P_{DC}}{1mW}) - P_{out} \tag{2.9}$$

in which the oscillator output power P_{out} is added. But FoM_{TP} is not fair when comparing oscillator cells with oscillator arrays. In an array, with coherent combining of the oscillator cells, the output power and phase noise performances get improved at the same time with the price of more dc power consumption.

While in (2.9), the dc consumption penalty is compensated by higher output power alone and the array can take the advantage of better phase noise. But in fact, any oscillator cell can be used to form an array, so it is more fair to calibrate out this advantage. To do that, a figure of merit FoM_{TE} is defined as:

$$FoM_{TE} = L(\Delta f) - 20\lg(\frac{f_0}{\Delta f}\frac{TR}{10}) + 10\lg(\frac{P_{DC}}{1mW}\frac{1}{\eta_{osc}}) \tag{2.10}$$

Instead of the oscillator output power, the dc-to-RF efficiency η_{osc} is added into the equation. With the proposed 210-GHz compact harmonic oscillator, a FoM_{TE} of -160.8 dBc/Hz is achieved, which is the best among all the state-of-the-art silicon-based oscillators in this band as shown in Table 2.1.

2.4 Conclusions

In this chapter, a device-centric bottom-up design methodology is described and used in the design of a 210-GHz harmonic oscillator prototype. Based on the parasitic tuning mechanism, a wide tuning range is also achieved without using low-quality lossy varactors. The propose compact surrounding passive network is capable of providing optimal terminations for the active devices within a wide frequency range, thus high output power and excellent dc-to-RF efficiency are achieved across the tuning range. The oscillator prototype also features good phase noise performance, which makes it very suitable to be integrated into THz systems. According to the performance comparison shown in Table 2.1, this oscillator achieves the best figure of merit among all the state-of-the-art silicon-based oscillators in this frequency band.

Table 2.1: Performance comparison with other state-of-the-art terahertz oscillators on silicon.

Reference	Frequency (GHz)	Output Power (dBm)	DC-to-RF Efficiency	Tuning Range	Phase Noise (dBc/Hz)	DC Power (mW)	Area (mm^2)	$\lvert FoM_{TE} \rvert$ [1]	Technology
ISSCC 2016 [36]	190.5	-2.1	0.21%	20.7%	-102.6 @ 10MHz	183 ~ 294	0.64 (Chip)	143.1	130-nm SiGe
TMTT 2013 [35]	212	-7.1	0.65%	2.8%	-92 @ 1MHz	30	0.073 (Core)	150.8	130-nm SiGe
ISSCC 2014 [33]	256	4.1	1.14%	6.5%	-94 @ 1MHz	227	0.44 (Chip)	155.4	65-nm CMOS
JSSC 2013 [37]	260	0.5 [2,3]	0.14% [2,3]	1.45%	-78 @ 1MHz	800	2.3 (Chip)	112.0	65-nm CMOS
JSSC 2012 [31]	280	-7.2 [3]	0.023% [3]	3.2%	-112 @ 10MHz	820	7.2 (Chip)	125.5	45-nm SOI
JSSC 2013 [32]	288	-1.5	0.3%	1.39%	-87 @ 1MHz	275	0.325 (Chip)	129.4	65-nm CMOS
JSSC 2012 [34]	290	-1.2	0.23%	4.5%	-78 @ 1MHz	325	0.36 (Chip)	128.8	65-nm CMOS
MWCL 2014 [39]	293	-2.74 [2,4]	2.76% [2,4]	5.74%	-93 @ 10MHz	19.2	0.258 (Chip)	149.1	65-nm CMOS
JSSC 2013 [40]	317	-13.3	0.07%	5%	-78 @ 10MHz	63	/	112.5	120-nm SiGe
This Work	210	1.4	2.4%	10.6%	-87.5 @ 1MHz	26 ~ 61	0.08 (Chip) 0.027 (Core)	160.8	130-nm SiGe

1. Defined in Equation (2.10). 2. Radiated power. 3. Silicon lens is used.
4. Measured with VNA extender and spectrum analyzer, not with power meter.

CHAPTER 3

FULLY-INTEGRATED HIGH-SENSITIVITY COHERENT TERAHERTZ IMAGER

Imaging is the most famous application for terahertz radiation, which has many potential applications in different areas, such as scientific researches, military and industrial production. In this chapter, a fully-integrated coherent THz imaging system is introduced.

3.1 Introduction to Terahertz Imaging Techniques

Due to the emerging applications in security screening [10], medical diagnostic [12], biology [14] and material characterization [18], terahertz imaging techniques are attracting increasing attentions. Compared to microwave frequencies, the shorter wavelength could effectively enhance the spatial resolution. Compared to X-ray, the non-ionizing nature makes it safer and more preferable in many applications. As the development of fabrication and design techniques, silicon platform is becoming more and more attractive and suitable for terahertz imagers implementation, since it could provide much higher integration level and yield, as a result, significantly lower cost and smaller size.

According to Planck's law of thermal radiation, terahertz wave is emitted from any warm body as part of the black-body radiation [41], but the emitted power is normally very weak. Due to the limited sensitivity of current silicon detectors, active imaging scheme is more practical, which means a high-power terahertz radiating source is needed for illumination. As a result, lots of research efforts were paid on silicon terahertz sources design and significant progress has

been made. In [31], a 280-GHz 4×4 radiating array capable of beam-steering is presented, which achieves a 0.19-mW output power and a 9.4-dBm EIRP. A 338-GHz 2-D 4×4 phased array is introduced in [42], the obtained output power and EIRP are 0.81 mW and 17.1 dBm, respectively. In [43], a 530-GHz source module with up to 1 mW output power for diffuse illumination is demonstrated. To form a complete imaging system, a terahertz detector is needed to pair up with the source. Previous works have also demonstrated terahertz detectors on silicon successfully. Using Schottky-barrier diodes, a 280-GHz 4×4 array and an 860-GHz detector cell are demonstrated, achieving minimum NEP of 29 $pW/\sqrt{Hz}$ and 42 $pW/\sqrt{Hz}$, respectively [24]. In [26], a 320-GHz 4×4 imaging array in a SiGe technology is presented, which is measured to have an average NEP of 34 $pW/\sqrt{Hz}$. In [25], a 1 k-pixel terahertz imaging camera chip at 860 GHz is introduced, which achieves an NEP of 100 $pW/\sqrt{Hz}$.

However, since most of the previous works are based on incoherent direct detection, the sensitivity is limited. Consequently, in order to obtain a reasonable dynamic range, normally an off-chip high-power source is needed for illumination [24]–[26]. In order to implement a fully-integrated terahertz imager, the detector sensitivity needs to be improved to alleviate the output power requirement on the source, so that an on-chip source would suffice. To enhance the detector sensitivity, the heterodyne detection scheme can be used [44]. However, this requires frequency coherency between the source and the detector. To achieve this, multiplier-chain based sources could be used, but they are normally less power efficient and need high power RF drive signals [29]. Fortunately, the phase-locked terahertz sources on silicon have been demonstrated recently. In [45], a 300-GHz phase-locked loop is introduced, which can provide a 40-μW probed output power. In [2], a 320-GHz transmitter chip with on-chip

phase-locked loop achieving a 3.3-mW output power and a 22.5-dBm EIRP is demonstrated.

In the rest of this chapter, design of a 320 GHz coherent imaging transmitter and receiver pair is presented. In the transmitter chip, a 4×4 radiator array is inject-locked to an on-chip phase-locked loop (PLL) to provide terahertz illumination. In the receiver chip, an 8-cell subharmonic-mixing detector array is used to perform a coherent heterodyne detection to enhance sensitivity. Even though coherent imaging has been demonstrated previously, all of them use multiplier-chain based sources [46] or inject-lock on-chip sources to outside signal [47], which all require high-frequency high-power RF inputs. Using the PLL-based structure, this work demonstrates the first fully-integrated coherent terahertz imaging transceiver on silicon.

3.2 Principles of Heterodyne Detection and the System Architecture

Due to the limited f_{max} and breakdown voltage of silicon transistors, obtaining high output power is still challenging. With the current on-chip silicon sources, in order to achieve high dynamic range for high quality imaging, the sensitivity of the detector needs to be enhanced.

3.2.1 Heterodyne Detection and Direct Detection

The conventional incoherent direct detection scheme is shown in Fig. 3.1(a). If an input signal $V_{RF}\cos(\omega_{RF}t + \varphi_{RF})$ is applied, the produced dc output change is written as $a_2 V_{RF}^2/2$, where a_2 is determined by the nonlinear device used. Due to its simplicity, this scheme is used in most of the previous works [24]–[26]. To alleviate the impact of the device flicker noise, the output signal is normally chopped to an IF frequency. As a result, the output IF signal (fundamental tone of the square wave after chopping) is:

$$V_{IF}(t) = \frac{1}{\pi} a_2 V_{RF}^2 \cos(\omega_{IF}t) \tag{3.1}$$

in which, ω_{IF} is the chopping frequency. In the heterodyne detection scheme, the input terahertz signal is mixed with a local oscillation (LO) signal to generate the output IF signal, as shown in Fig. 3.1(b). In this case, if a terahertz input of $V_{RF}\cos(\omega_{RF}t + \varphi_{RF})$ and LO of $V_{LO}\cos(\omega_{LO}t)$ are applied, the output IF signal is:

$$V_{IF}(t) = -b_2 V_{RF} V_{LO} \cos(\omega_{IF}t + \varphi_{RF}) \tag{3.2}$$

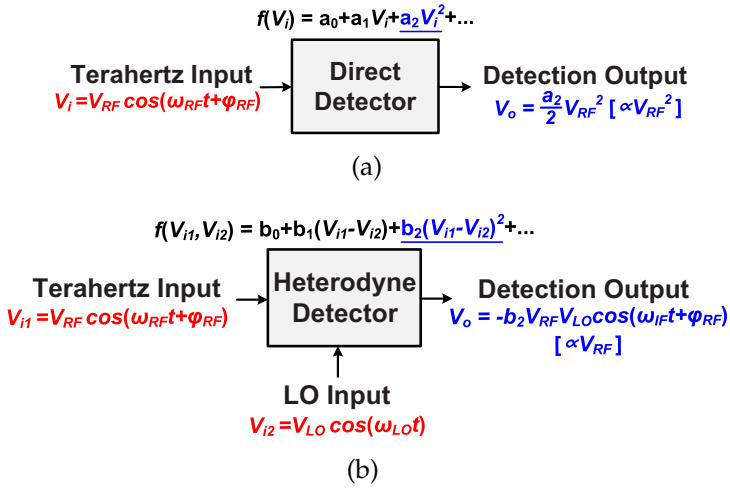


Figure 3.1: Principles of (a) incoherent direct detection and (b) coherent heterodyne detection.

in which, ω_{IF} equals to the frequency difference between the RF and LO; φ_{RF} represents the phase of the RF signal; b_2 is the mixing coefficient of the device. Comparing (3.1) and (3.2), we can see that, in the heterodyne detection case:

(i) The output drops with V_{RF} instead of V_{RF}^2, meaning when the RF signal is weak, output of a heterodyne detector drops much slower compared to a direct detection one.

(ii) The output signal is also proportional to V_{LO}. Normally, as the LO power is considerably higher than the RF signal, the output signal will also be stronger.

(iii) Phase information of the RF signal (φ_{RF}) is preserved at the output. As a result, electrical scanning based on digital beam forming is achievable, which has the potential to replace the traditional mechanical scanning to significantly reduce the imaging time.

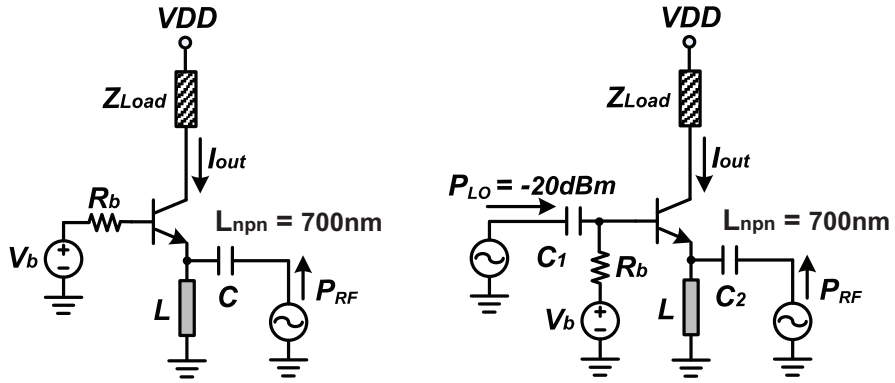


Figure 3.2: The STMicroelectronics 0.13-μm BiCMOS bipolar transistor with a 700-nm emitter length configured as (a) direct detector and (b) heterodyne detector.

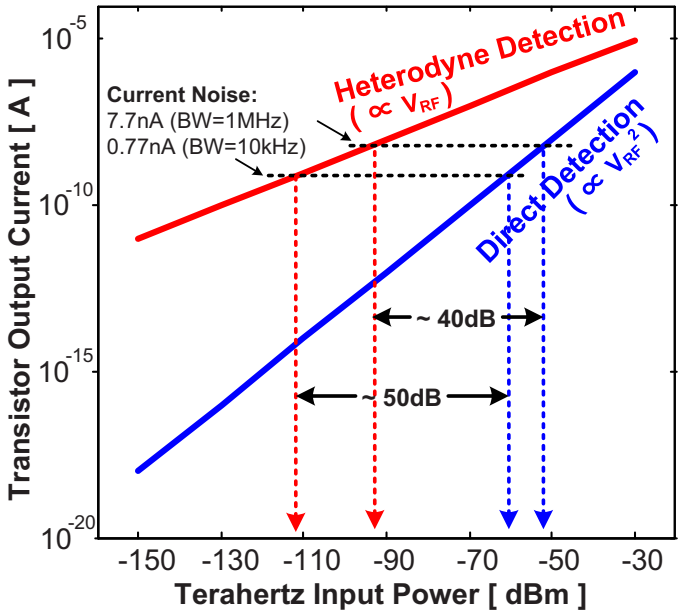


Figure 3.3: Comparison simulation results using the STMicroelectronics 0.13-μm BiCMOS bipolar transistor.

Therefore, the heterodyne detection scheme can largely enhance the detector performance. For a further comparison, a bipolar transistor is configured both as a direct detector (input power injected from the emitter, as shown in Fig. 3.2(a)) and a heterodyne detector (input power injected from the emitter and -20dBm LO power pumped into the base, shown in Fig. 3.2(b)). The simulated output current with different RF power in both cases is shown in Fig. 3.3. It is obvious that under low RF power, which is the real scenario in most applications, the heterodyne detection scheme shows a great advantage. With an assumed bandwidth of 1 MHz, the simulated integrated current noise is 7.7 *nA*. Under this circumstance, to achieve a signal-to-noise ratio (SNR) of 1, the required input power for the heterodyne detector is around 40 dB lower than the direct detector. If a bandwidth of 10 kHz is chosen, the difference becomes 50 dB, as shown in Fig. 3.3.

3.2.2 Subharmonic-Mixing Heterodyne Transmitter and Receiver Architecture

The heterodyne detection scheme requires frequency coherency between the transmitter and the receiver in order to obtain an output signal with a stable frequency. Frequency coherency can be obtained by using multiplier chains, however it has two obvious drawbacks: (i) it needs high-power high-frequency drive signals, which normally come from off-chip sources; (ii) the dc-to-RF efficiency is normally low compared to oscillator-based sources [29]. In order to achieve higher integration level and better power efficiency, a PLL-based transceiver architecture shown in Fig. 3.4 is proposed. In the transmitter, the 320-GHz radiator is inject-locked to a 160-GHz PLL. There is one important issue that needs to be addressed: the radiator is required to generate high output power, which needs the oscillators in the radiator to have a large oscillation activity. However, the power injected into the radiator is limited due to the power consumption restriction of the PLL. As a result, the radiator can only be locked within a limited range near its free-running frequency [49]. Fortu-

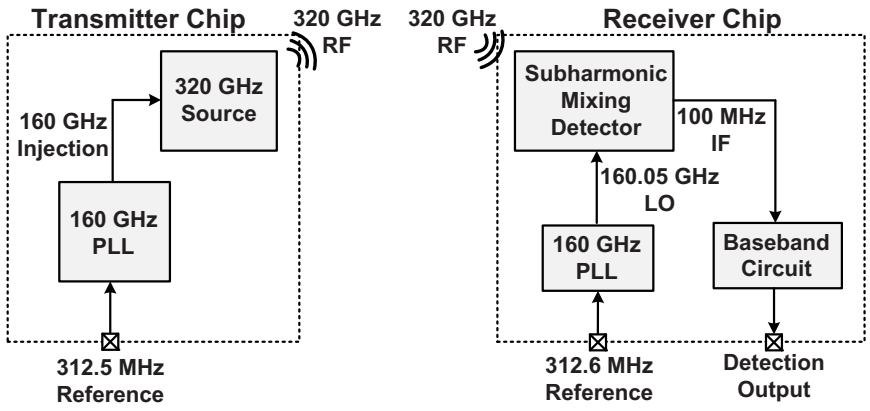


Figure 3.4: The PLL-based subharmonic-mixing heterodyne-detection transmitter and receiver architecture.

nately, the heterodyne detection scheme does not require large frequency tuning. However, since the free-running frequency of the radiator is hard to predict accurately due to the inaccurate device model at high frequency and process variation, the PLL needs to have a sufficient tuning range to cover the possible frequency shift of the radiator. In the receiver, the phase-locked 320-GHz RF signal is mixed with the 160.05-GHz LO generated by the receiver PLL. Ideally, we could use the PLL to inject-lock another 320-GHz oscillator to generate the LO signal. However, with a large oscillation activity in the 320-GHz oscillator, the tuning range for the LO is largely reduced as discussed before. Due to the possible frequency mismatch caused by process variation between the transmitter and receiver, such small locking range may not be able to ensure frequency coherency. To address this issue, even with a relatively larger conversion loss, the subharmonic-mixing scheme is still used to obtain a wider LO tuning range to ensure frequency coherency. Moreover, in this scheme, the PLL in the transmitter can be reused in the receiver with minor modifications, which makes it much simpler and also causes less frequency mismatch. After the subharmonic mixing, the output 100-MHz IF signal is then processed by the on-chip baseband circuits. The detection output is finally collected and sent to a computer for image construction.

3.3 Design of the High-Power Phase-Locked Transmitter

Even though the heterodyne detection scheme could enhance the sensitivity of the detector, it is still desirable to achieve high output power for better SNR and image quality. Shown in Fig. 3.5 is the architecture of the high-power 320-GHz phase-locked transmitter. Sixteen radiator cells form a 4×4 radiator array

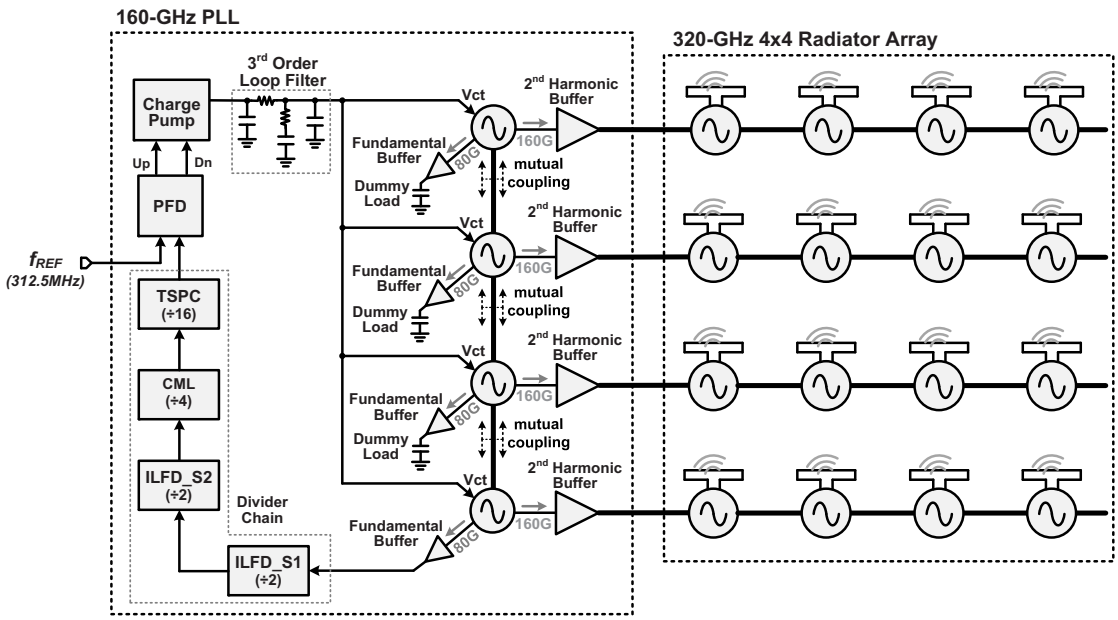


Figure 3.5: The high output power 320-GHz phase-locked transmitter architecture.

with their power adding up in free space. The radiator array is then injection-locked by the 160-GHz PLL. A similar design was published previously [3], however, only 200 MHz tuning range is achieved at the 320-GHz output. It will be shown later that, patch antennas are used on the receiver side, which have a narrow bandwidth. In order to ensure the transmitted frequency falls inside the receiver antenna bandwidth, a much larger frequency tuning range is desired. Next, design details of some critical circuit blocks are given.

3.3.1 The Radiator Array

Since the targeted frequency is higher than the f_{max} of the transistors in this 0.13-μm BiCMOS process (f_{max} = 280 GHz [50]), harmonic oscillators are used. It has been shown in [37] that, there are several conditions for maximizing the

radiated harmonic power:

(i) As already discussed in Chapter 2, if a bipolar transistor is represented using a two-port network, as shown in Fig. 2.3, there is an optimum phase condition for the complex collector-to-base voltage gain, A, to maximize the fundamental oscillation activity: $\angle A_{opt} = \angle - (y_{21} + y_{12}^*)$.

(ii) Also mentioned in Chapter 2, isolation between the transistor base and collector at the second harmonic is necessary to eliminate the self-power-cancellation/loading effect.

(iii) Isolation between the transistor base and collector at dc for separate biasing.

(iv) Efficient harmonic-signal radiation near the transistor is desired in order to avoid additional feed line or matching network loss.

Two adjacent radiator cells used in this design are shown in Fig. 3.6, in which a similar return-path-gap coupler (RPGC) based self-feeding oscillator structure discussed in Chapter 2 is used. The self-feeding lines are used to achieve the optimum phase condition for the transistors. Also, since the RPGC is opaque to even-mode signals, isolation between the base and collector at the second harmonic is achieved. The RPGC also naturally separates the dc, which allows us more freedom for optimal base and collector biasing. One big difference from the oscillator design shown in Chapter 2 is that, in order to instantly radiate the generated second harmonic power, the top slots are folded to shape a folded half-wavelength slot antenna, as shown in Fig. 3.6. Overall, all the aforementioned conditions are met simultaneously in this radiator design, which helps to generate maximum radiated harmonic power.

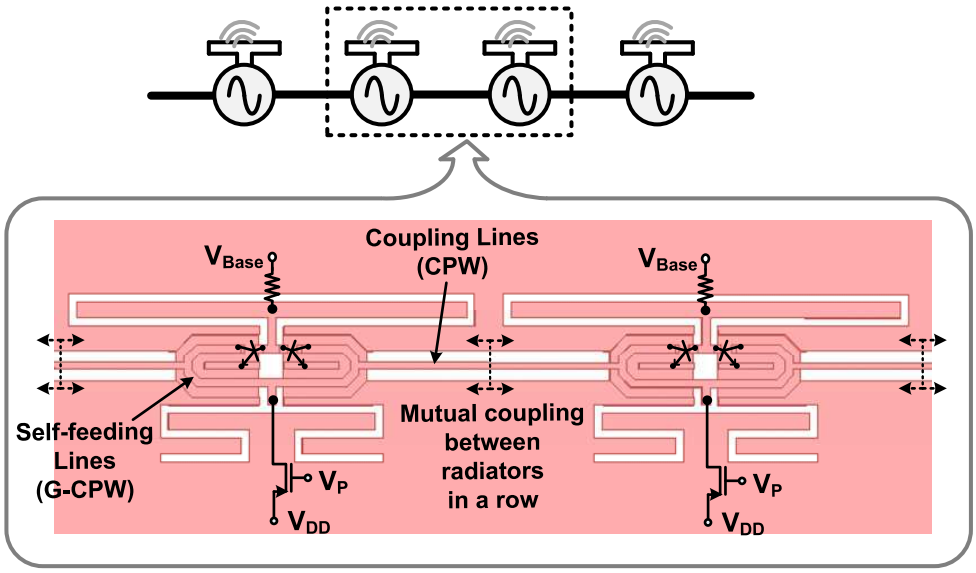
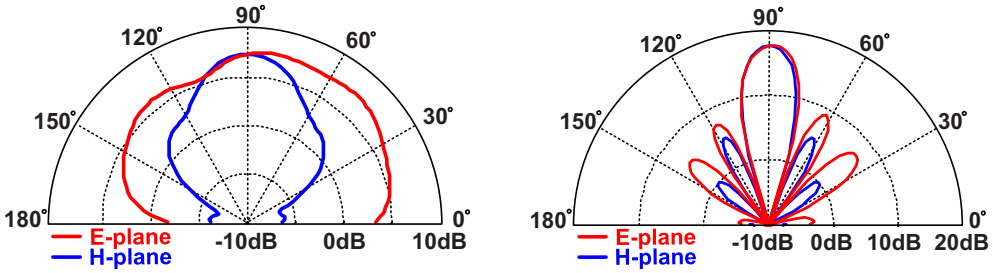


Figure 3.6: The radiator cells and coupling between them.

To increase the total radiated power, sixteen radiator cells are implemented to form a 4×4 array with their power combining constructively in the far field, as shown in Fig. 3.5. In each row, four radiator cells are mutually coupled together. The mutual coupling is realized through coupling transmission lines tapping on the radiator self-feeding lines, as shown in Fig. 3.6. In [3], it has been shown that the radiator cells can only be coupled in-phase, so the boundary between two adjacent cells behaves like an open termination. As a result, the added coupling lines act like small shunt capacitors. To minimize the impact, the coupling lines need to be short and have a high characteristic impedance. As a result, CPW lines with thin signal traces are used. Due to the compact design of the radiator cells, the 4×4 array only occupies an area of 0.87×0.85 mm^2. The simulated backside radiation patterns of a single radiator and the 4×4 array are shown in Fig. 3.7, with a directivity of 7.4 dBi and 17.7 dBi, respectively.



(a) (b)

Figure 3.7: Simulated radiation pattern of (a) one radiator cell and (b) the 4×4 array.

3.3.2 The 160-GHz Phase-Locked Loop

As shown in Fig. 3.5, the PLL is composed of a phase-frequency detector (PFD), a charge pump (CP), a 3^{rd}-order loop filter, a divide-by-256 divider chain and four mutually-coupled VCOs as well as VCO fundamental buffers and harmonic buffers.

Since there is no strong coupling mechanism among the radiator rows, four mutually-coupled VCOs are implemented to inject their second harmonic into each radiator row to obtain overall synchronization. The schematic of the VCO with the fundamental buffer is shown in Fig. 3.8. As mentioned before, to assure frequency locking between the PLL and the radiator array, a large tuning range is required for the PLL. However, in conventional cross-coupled VCOs, the large transistor parasitic capacitance C_π is in parallel with the varactor, which makes it extremely hard to get a desired tuning range with adequate oscillation power due to the lossy varactor at this frequency. To obtain a better tradeoff, a differential Colpitts oscillator topology is adopted [3]. In the VCO, a common-base cascode stage (Q_3 and Q_4) is placed on top of the main transistors Q_1 and Q_2 to provide a low-impedance termination required by Colpitts oscillators. The second

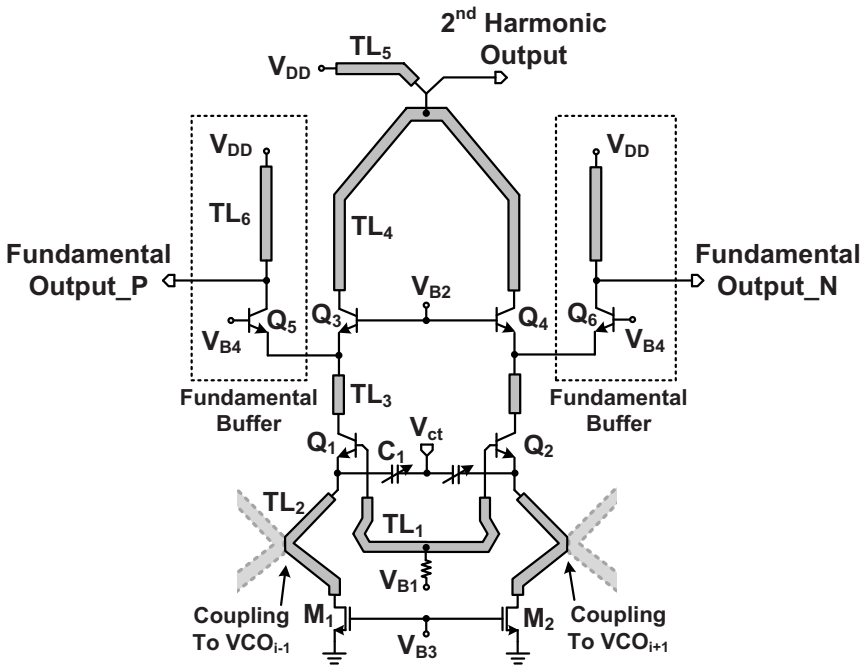


Figure 3.8: Schematic of the VCO and the fundamental buffer.

harmonic signal is extracted at the top of the transmission line TL_4, which will be sent to the second harmonic buffer. The transmission line TL_2 is used to transform the large parasitic drain capacitance of M_1 and M_2 into a weakly inductive impedance, so the operation of the VCO is not affected. The intermediate node of TL_2 is directly connected to the adjacent VCO for a strong mutual coupling. Similar to the mutual coupling of the radiators, VCOs are coupled in-phase and the connect points present open, so each VCO itself is not affected. The control signal (V_{ct} , shown in Fig. 3.5) is carefully distributed into the four VCOs to avoid frequency mismatch. Another common-base NPN transistor pair Q_5 and Q_6 with transmission lines on their collectors form the differential fundamental buffer, which feeds the 80-GHz output fundamental signal into the following divider chain (or dummy load, for minimizing frequency mismatch among the VCOs). Shown in Fig. 3.9 is the second harmonic buffer, a cascode structure is used. A series L and C section is placed at the base of Q_2, which resonate at

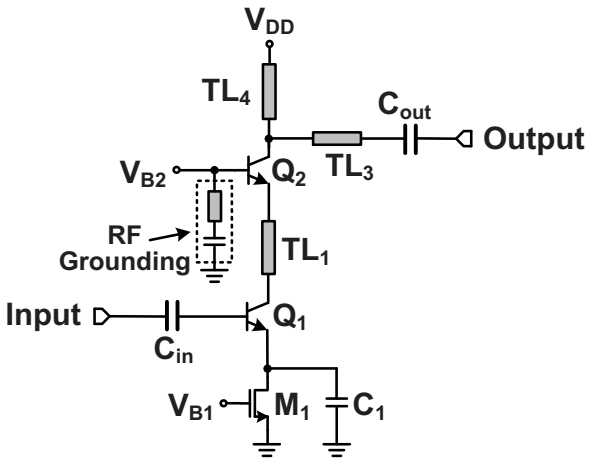


Figure 3.9: Schematic of the VCO second harmonic buffer.

160 GHz to present a small impedance for RF grounding. Both input and output coupling capacitors (C_{in} and C_{out}) are custom designed metal-oxide-metal capacitors to get a higher quality factor and minimize the parasitic capacitance to the ground. According to simulation, -2.4 dBm power is injected into each radiator row from the second harmonic buffer. It is worthy to mention that, in steady state, the loading of the second harmonic buffers will break the symmetry of the radiator rows. In order to minimize this impact, the buffers need to have large output impedances.

Shown in Fig. 3.10 is the schematic of the injection-locking dividers (ILFDs). The transmission line TL_1 and transistor pair Q_1 and Q_2 form the oscillator core of the first-stage ILFD. The free-running frequency is designed to be 40 GHz and can be tuned by changing the bias of the tail NMOS transistor M_1 in case of process variation. The input signal is injected into the oscillator core through M_2 and M_3. For the second-stage ILFD, inverter based ILFD topology is used for its compact size and wide locking range. Multi-phase injection technique is also adopted to further increase the locking range [51]. Eventually, the overall input

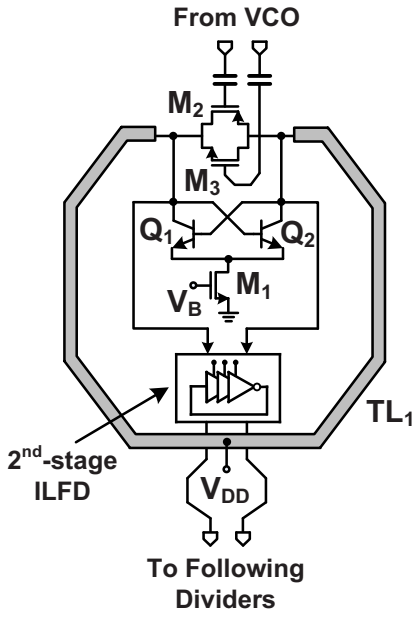


Figure 3.10: Schematic of the injection-locking dividers.

locking range of the ILFDs is determined by the first stage, which is simulated to be from 75 GHz to 85.2 GHz, and is large enough to ensure locking of the whole PLL. Output of the ILFDs is sent to two cascaded CML dividers (20 GHz to 5 GHz) followed by a divide-by-16 digital divider made of TSPC logic (from 5 GHz to 312.5 MHz). The total division ratio of the divider chain is 256.

Finally, the simulated locking range of the PLL is around 17 GHz at the 160-GHz output, which is large enough to cover ±5.3% radiator frequency shift. This is very helpful for assuring frequency coherency even under large process variation.

3.4 Design of the High-Sensitivity Heterodyne-Detection Receiver

To pair with the transmitter, a 320-GHz high-sensitivity subharmonic-mixing coherent receiver is designed, with the architecture shown in Fig. 3.11. It is

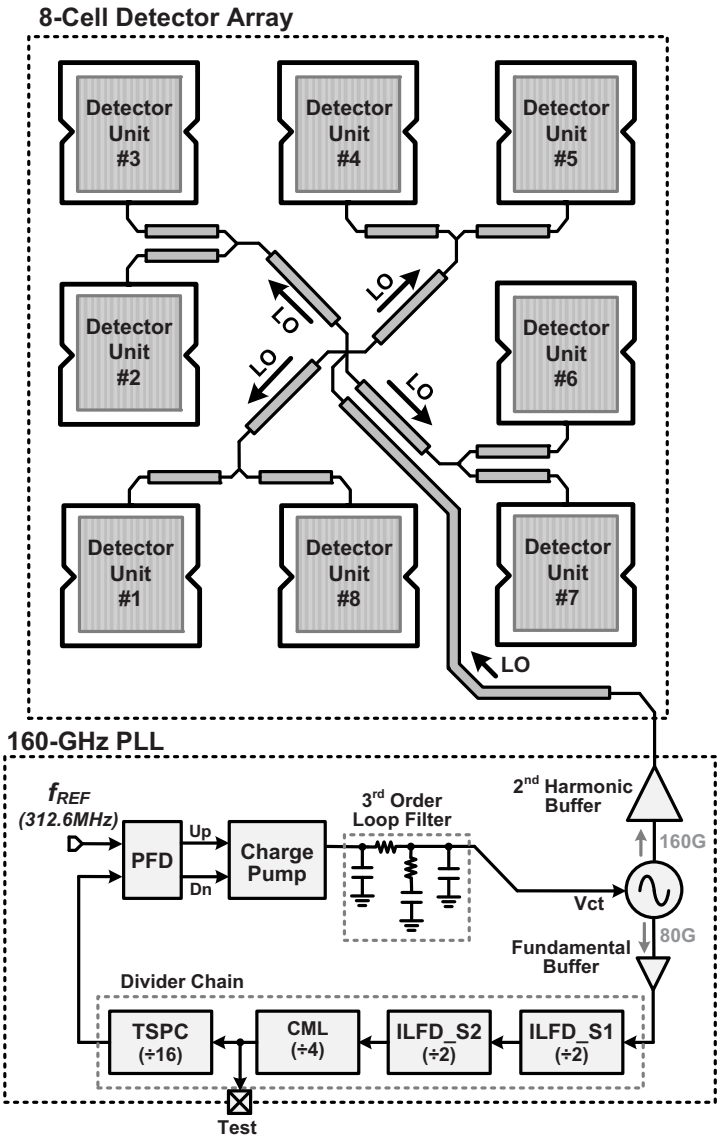


Figure 3.11: The subharmonic-mixing heterodyne-detection receiver architecture.

composed of an 8-cell detector array, a 160-GHz PLL and an LO distribution network. Using the subharmonic-mixing scheme, the output of the PLL is directly used as the LO signal. In this way, a lower power consumption and much wider LO tuning range is achieved. In this section, some design details will be discussed.

3.4.1 The Subharmonic-Mixing Heterodyne Detector Cell

The structure of the proposed subharmonic-mixing heterodyne detector cell is shown in Fig. 3.12, in which bipolar transistors are used to perform the LO and RF mixing. The received RF signal is injected to the emitter of the transistors and the LO signal is fed from their base. The detector cell is made into a differential form in order to alleviate the LO self-mixing problem. After LO and RF mixing, the generated IF signal is amplified by a low noise pre-amplifier before it gets mixed again into the 100-kHz baseband signal. Finally a low-pass filter with a 200-kHz cutoff frequency is followed to filter out the unwanted components.

To accommodate the differential detector structure, a differential patch antenna is designed. The top and cross section views of the antenna are shown in Fig. 3.13(a) and (b). The antenna occupies an area of $250 \times 240\ \mu m^2$. The antenna is implemented using the top metal (M6), which has a thickness of 3 μm. To avoid the terahertz wave from coupling into the lossy silicon substrate, an overlapped M1-to-M3 ground plane is placed underneath the antenna. The distance between the antenna to the ground plane is 7.61 μm. To avoid cross-talking with the near-by structures (transmission lines, transistors, etc.), stacked M1-to-M6 metal walls are placed surrounding the antenna with a 20-μm clearance.

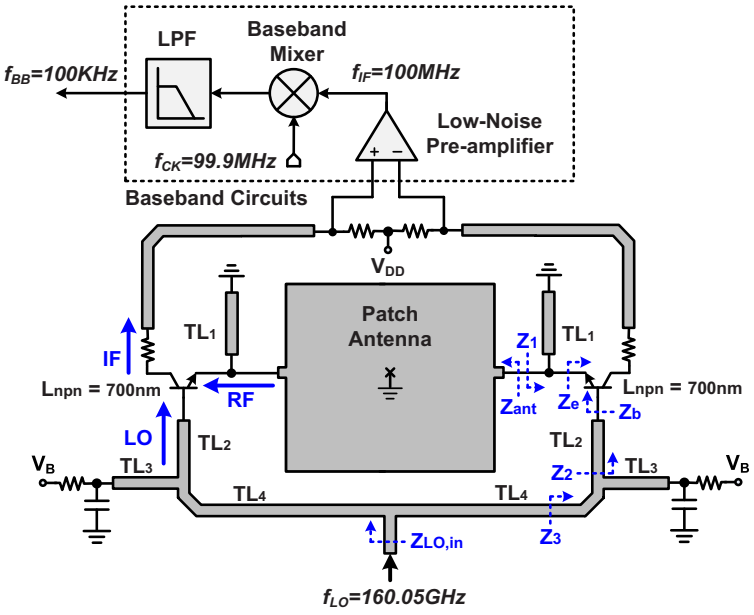


Figure 3.12: Structure of the subharmonic-mixing heterodyne detector cell.

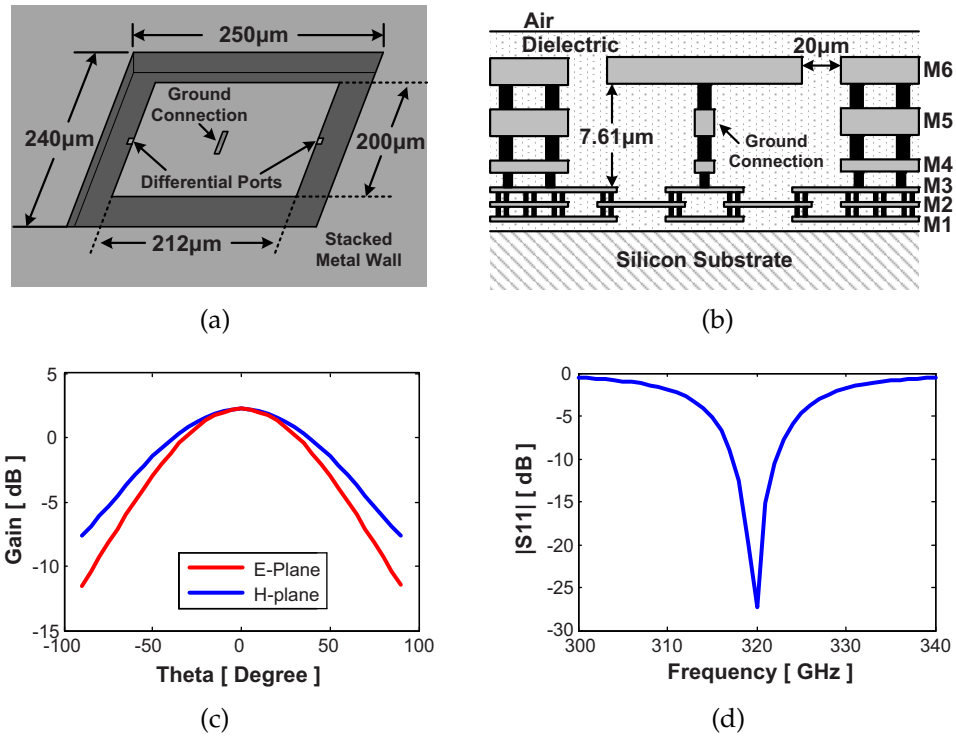
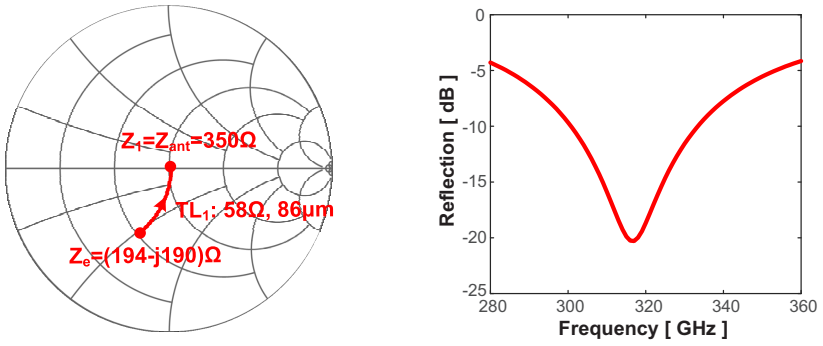


Figure 3.13: The differential patch antenna: (a) top view (b) cross section (c) simulated antenna gain in different directions and (d) simulated reflection coefficient versus frequency (Z_{in} = 350Ω).

Though the ground walls slightly degrade the efficiency of the antenna, adding them provides us with better prediction of the antenna resonance frequency, which is very important due to the narrow bandwidth of the patch antennas. As shown in Fig. 3.12, the emitter of the transistors is directly connected to the antenna. To provide a dc bias, the center of the patch antenna is connected to ground as shown in Fig. 3.13(a) and (b). Due to the differential structure, central line of the antenna is equivalently RF grounded, so this ground connection has no impact. The length of the antenna is set to be 212 μm for a resonance at 320 GHz, and the width is designed to be 200 μm to obtain an impedance of 350 Ω for easy matching with the input impedance at the emitter. The simulated antenna gain in different directions as well as the reflection coefficient versus frequency are shown in Fig. 3.13(c) and (d). The antenna gain in the broadside is simulated to be 2.2 dB.

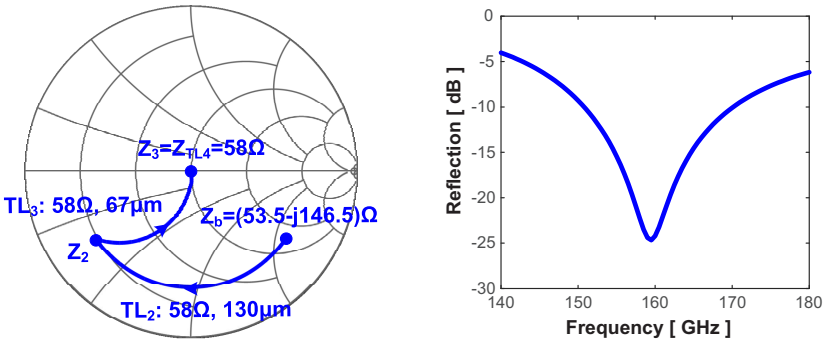
To minimize the RF signal loss, the transistors are placed as close to the antenna as possible, with a very simple matching scheme: only one shunt transmission line stub (TL_1) is used as shown in Fig. 3.12. The matching scheme on a smith chart is shown in Fig. 3.14(a). The 86-μm shunt stub TL_1 transforms



(a) (b)

Figure 3.14: RF matching at emitter: (a) matching scheme on a smith chart and (b) simulated reflection coefficient versus frequency.

the emitter impedance of (194-j190) Ω into 350 Ω for matching with the patch antenna. To make this matching scheme feasible, a co-design is needed for the antenna and the transistors in order to obtain suitable impedances. Beside that, a trade-off between the conversion loss and the device noise also needs to be considered while choosing the transistor size. Simulation result of the RF reflection coefficient at the transistor emitter (assuming a source impedance of 350 Ω) is shown in Fig. 3.14(b). In the detector cell, all the transmission lines are made of G-CPW lines with characteristic impedance of 58 Ω. The matching scheme for the LO signal is shown in Fig. 3.15(a). The transmission line section TL_2 and the short matching stub TL_3 transform the capacitive transistor base input impedance into a 58-Ω impedance, so that it is perfectly matched with the characteristic impedance of the feed line TL_4. The dc bias for the base of the transistors is provided at the far end of TL_3. Then, the feed lines (TL_4) on the two sides combine to form a common LO feed-in point, which has an input impedance ($Z_{LO,in}$) of 29 Ω. The simulated LO reflection coefficient at this feed-in point (assuming a source impedance of 29 Ω) is shown in Fig. 3.15(b).



(a) (b)

Figure 3.15: LO matching at base: (a) matching scheme on a smith chart and (b) simulated reflection coefficient versus frequency.

3.4.2 The 160-GHz Phase-Locked Loop

The PLL in the receiver is very similar to the one in the transmitter, but it has only one VCO, as shown in Fig. 3.11. Also, high output impedance is no longer required for the VCO second harmonic buffer, so it can be modified to maximize the delivered LO power. The simulated output tuning range is 18.1 GHz at the 160 GHz output, which is slightly larger than the one in the transmitter.

3.4.3 The Highly-Symmetrical LO Distribution Network

As shown in Fig. 3.11, the LO signal generated by the PLL needs to be delivered into each of the 8 detector cells. However, to distribute the LO power evenly with the same delay (phase) and power is challenging. In order to achieve that, a highly-symmetrical distribution network shown in Fig. 3.16 is designed. First, the LO feed-in points of every two adjacent detector cells are combined together with two S1 blocks, forming four adjoint points. Then, four S2 blocks combines the four newly formed adjoint points together to get a common LO feed-in point for all the 8 detector cells. Since the network is mainly built up upon S1 and S2 as well as their flipped and rotated versions, it is highly symmetrical, which is very helpful for the 8 detector cells to receive an LO signal with the same power and phase.

In the S1 block, a 38-Ω quarter-wave line transforms the 29-Ω detector cell LO port impedance into a 50-Ω impedance ($Z_1 = 50\Omega$). After two adjacent detector LO ports are combined, the impedance seen from each of the adjoint points will be: $Z_2 = Z_1/2 = 25\Omega$. Then, in the S2 block, another 38-Ω quarter-wave line TL_2 transforms Z_2 into an 60 Ω, so the length of the following 60-Ω line TL_3 can

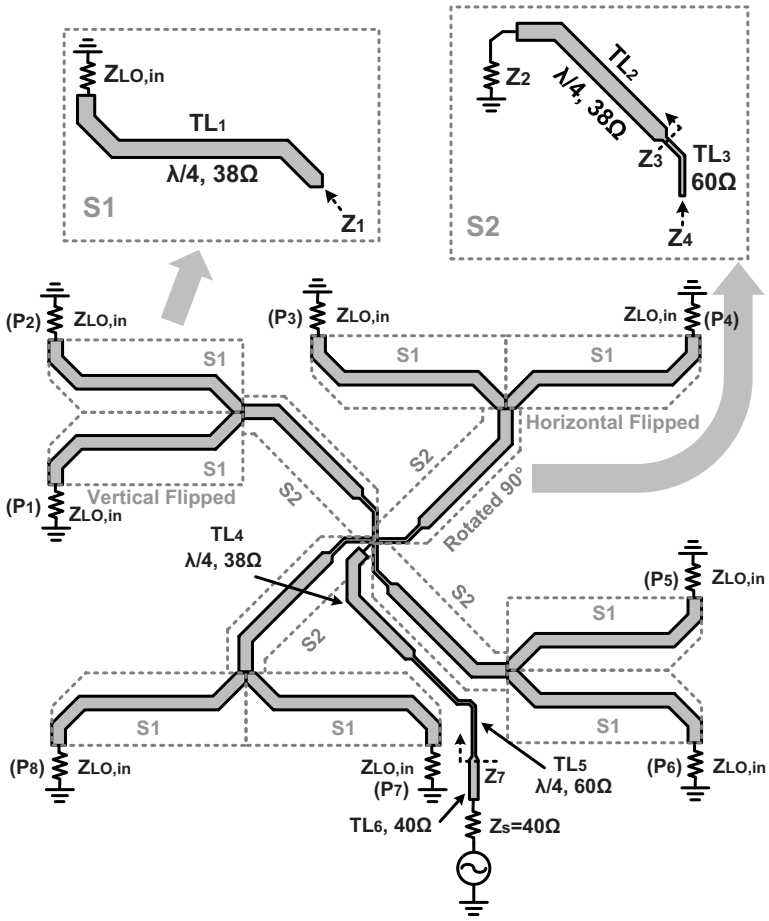


Figure 3.16: The highly-symmetrical LO distribution network structure.

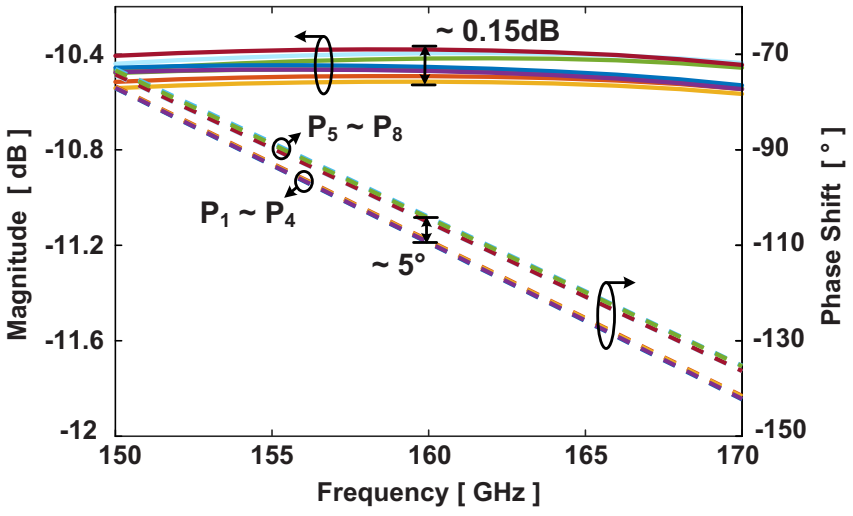
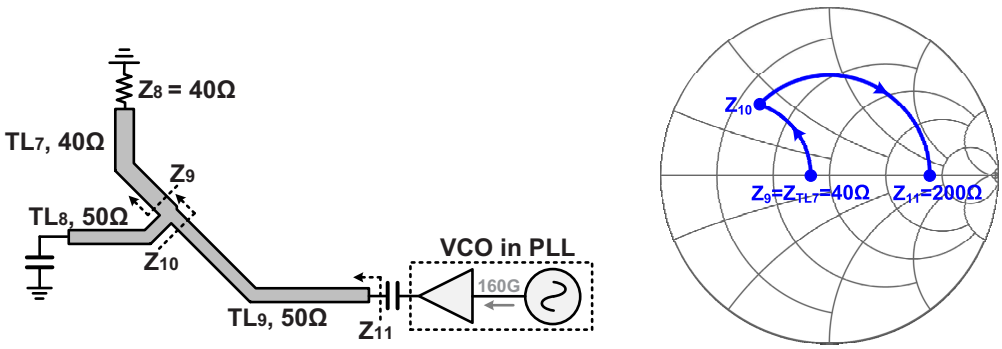


Figure 3.17: Simulation results of the LO distribution network.

be adjusted according to the desired distance between the detector cells. After the four S2 blocks join together, the impedance seen at the common LO feed-in point will be: $Z_5 = Z_4/4 = 15\Omega$. Then, a 38-Ω and a 60-Ω quarter-wave line (TL_4 and TL_5) further transform the impedance to 40 Ω ($Z_7 = 40\Omega$), as shown in Fig. 3.16. Assuming 0 dBm signal power is applied at the input port of the distribution network, the simulated power and phase shift at all the 8 output ports are shown in Fig. 3.17. The LO power is evenly distributed with only 0.15 dB difference among 8 output ports. The total loss of this distribution network is 1.5 dB. Phase of the upper 4 outputs ($P_1 \sim P_4$ in Fig. 3.16) is around 5° behind the lower 4 outputs ($P_5 \sim P_8$), this is because the transmission line tapping to the center of the network (TL_4 in Fig. 3.16) slightly breaks the symmetry. Fortunately, this phase difference only causes a constant phase offset, which can easily calibrated.

The simulated optimal load for the VCO harmonic buffer is 200-Ω, so a short stub matching structure is used to transform the 40-Ω input impedance of the LO distribution network to 200 Ω, as shown in Fig. 3.18. The 40-Ω feed line between the LO distribution network and this matching structure can have an



(a) (b)

Figure 3.18: Matching network at the output of the 160-GHz PLL: (a) structure and (b) matching scheme on a smith chart.

arbitrary length, providing more freedom for floorplan of the whole chip. Finally, the LO power delivered into each detector cell is simulated to be -12 dBm.

3.5 Experimental Results

The proposed coherent imaging transmitter and receiver chips are fabricated using the STMicroelectronics 0.13-μm SiGe:C BiCMOS process. The transmitter chip is shown in Fig. 3.19, which occupies an area of 1.6×1.3 mm^2. The receiver chip is shown in Fig. 3.20, which takes an area of 1.7×1.8 mm^2.

3.5.1 The Transmitter Performance Characterization

Since the transmitter chip radiates from the backside, to eliminate the lossy substrate wave, a high-resistivity hemispherical silicon lens is used [37]. For ease of packaging and alignment, a high resistivity silicon wafer (300 μm thick and

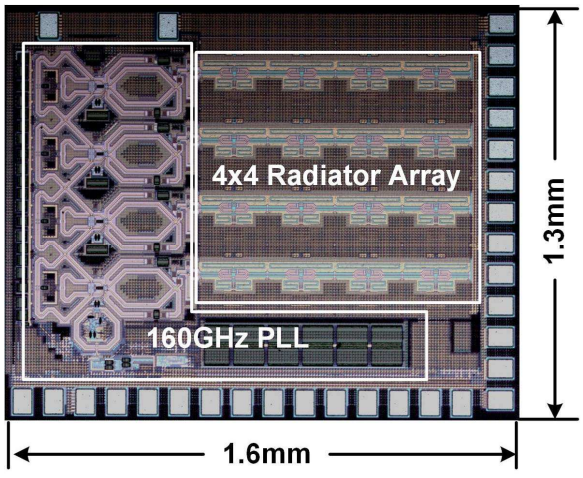


Figure 3.19: The microphotograph of the transmitter chip.

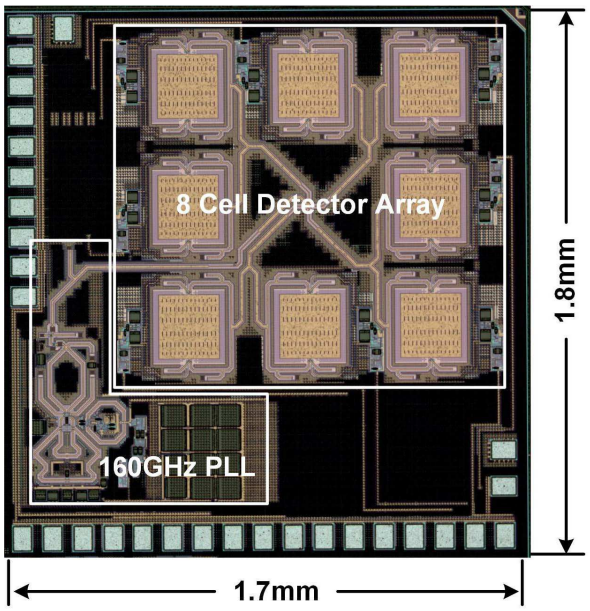


Figure 3.20: The microphotograph of the receiver chip.

$\sim$ 1 cm^2 large) is placed in-between the chip and the silicon lens [3]. The frequency/spectrum measurement setup is shown in Fig. 3.21(a), in which, an even harmonic mixer (EHM) mixes the received THz beam with the 16^{th} harmonic of the 20-GHz signal supplied by the signal source. The IF product is then measured with the spectrum analyzer. The measured IF spectrum with the PLL on and off is shown in Fig. 3.22. When the PLL is off, there is no strong coupling among the radiator rows, multiple peaks are observed [Fig. 3.22(a)]. The number of the peaks does not equal to the number of the radiator rows, which is caused by the mutual pulling among the rows through the silicon substrate and antenna coupling. When the PLL is turned on, the radiator rows get synchronized through the mutually-coupled VCOs, and only a single peak is observed [Fig. 3.22(b)]. For a better comparison, a close-in spectrum of the free-running scenario and frequency locked scenario are plotted in the same graph, as shown in Fig. 3.23. It is obvious that, after the frequency locking, the spectrum of the

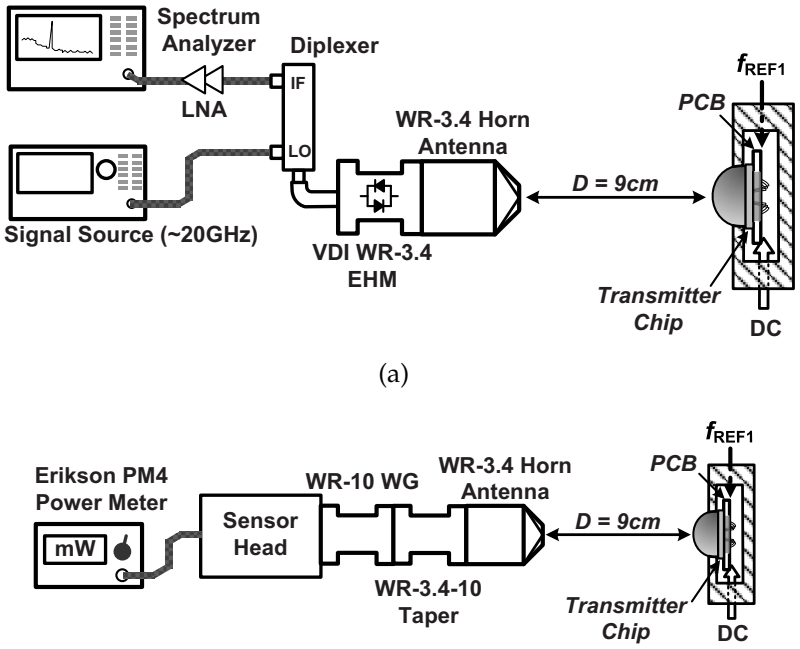
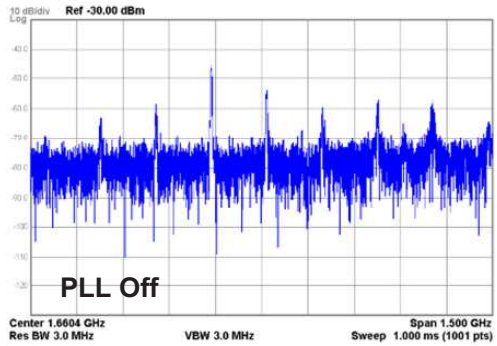


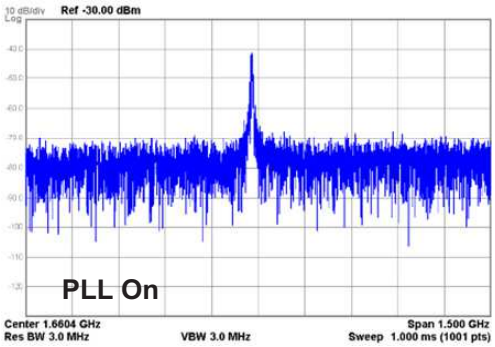
Figure 3.21: The transmitter measurement setups: (a) frequency measurement setup and (b) power measurement setup.

radiated THz beam is determined by the PLL, which presents a much sharper tone compared to the free-running case. The phase noise after the frequency locking is also shown in Fig. 3.23. Due to the large division ratio (N=1024 from 312.5 MHz to 320 GHz) and the wide tuning range requirement for the PLL, the output phase noise is sacrificed. The measured in-band (100 kHz offset) and out-of-band (10 MHz offset) phase noise is -67.4 dBc/Hz and -87.2 dBc/Hz, respectively. The frequency locking range of the transmitter under different radiator base bias voltages is shown in Fig. 3.24. As the bias voltage increases, the oscillation activity of the radiators also increases, and as discussed before, the locking range decreases quickly. However, a total locking range of 3.91 GHz is still achieved.

The radiation pattern of the transmitter shown in Fig. 3.25 is measured by ro-



(a)



(b)

Figure 3.22: Measured spectrum of the down-converted transmitter radiation when: (a) PLL is off and (b) PLL is on.

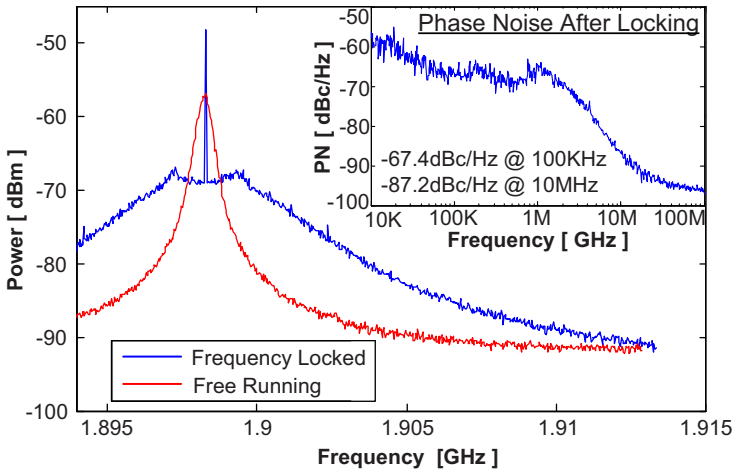


Figure 3.23: Close-in free-running and frequency-locked spectrum of the down-converted transmitter radiated signal and the phase noise of it after frequency locking.

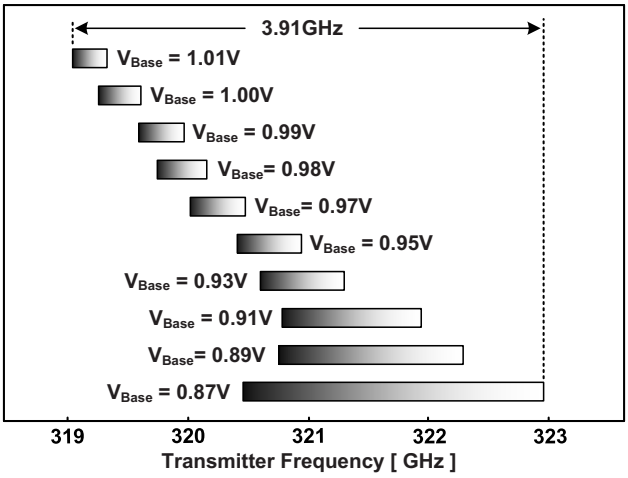


Figure 3.24: Measured frequency locking range under different radiator bias points.

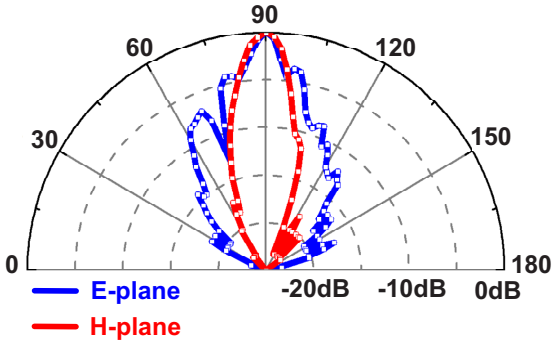
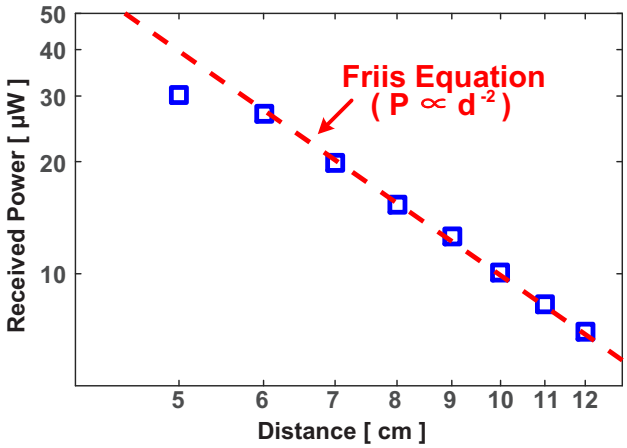
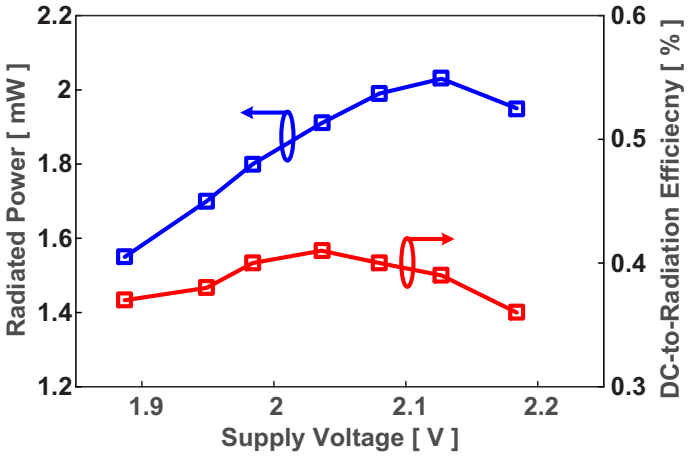


Figure 3.25: The measured radiation pattern of the transmitter.

tating the chip in both azimuth and elevation directions on a rotary stage. The measured directivity is 18.0 dBi. It is noteworthy that, insertion of the silicon wafer makes the chip not exactly at the spherical center of the lens, which will lead to beam collimation. This explains why we observe lower side lobe level in Fig. 3.25 compared to the simulation in Fig. 3.7(b). However, due to the concentrated beam radiated by the radiator array, the measured directivity is still close to the simulation [3]. The power measurement setup is shown in Fig. 3.21(b), in which a PM4 calorimeter is used for better precision. To obtain accurate re-



(a)



(b)

Figure 3.26: Power measurement: (a) measured power by the calorimeter at different distances from the transmitter chip and (b) measured peak output power and the associated dc-to-THz radiation efficiency under different supply voltages.

sults, we need to make sure the horn antenna is put far away enough from the transmitter to ensure far-field condition and avoid standing wave effect so that the Friis equation is valid. First, the distance is changed from 5 cm to 12 cm, the calorimeter measured power is shown in Fig. 3.26(a). It can be seen that, when the distance is larger than 6 cm, the results match with the Friis equation well. In the following measurements, a 9-cm distance is chosen. The supply voltage

for the transmitter is swept, and the peak radiated power as well as the associated dc-to-THz-radiation efficiency are shown in Fig. 3.26(b). The maximum radiated power and EIRP achieved are 2 mW and 21.1 dBm, respectively. The maximum dc-to-THz-radiation efficiency is 2.4%.

The transmitter chip consumes a total dc power of 605 mW: the radiator array dissipates 433 mW, the VCO array (including fundamental buffers and harmonic buffers) takes 128 mW and the rest of the PLL consumes a 44-mW power.

3.5.2 The Receiver Performance Characterization

The measurement setup for the receiver is shown in Fig. 3.27. The transmitter chip works as the source to radiate the 320-GHz RF signal. To eliminate the standing wave effect caused by reflection at the receiver PCB, an absorber is positioned in front of it with a hole for the wave to pass through. Even with the absorber, the receiver still needs to be put at least 15 cm away from the transmitter. The signal analyzer and the oscilloscope are used to observe the receiver

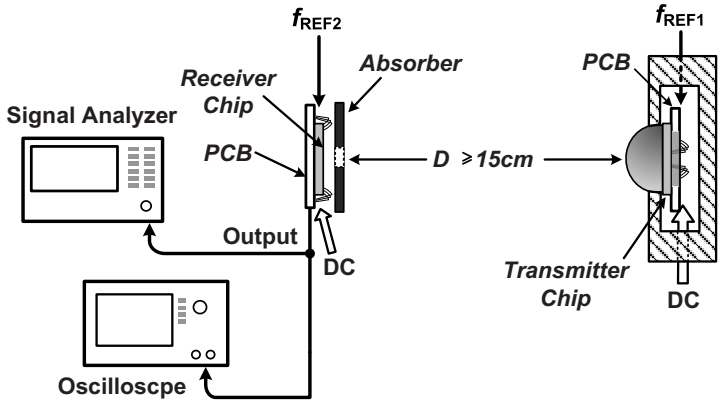


Figure 3.27: The measurement setup for the receiver chip.

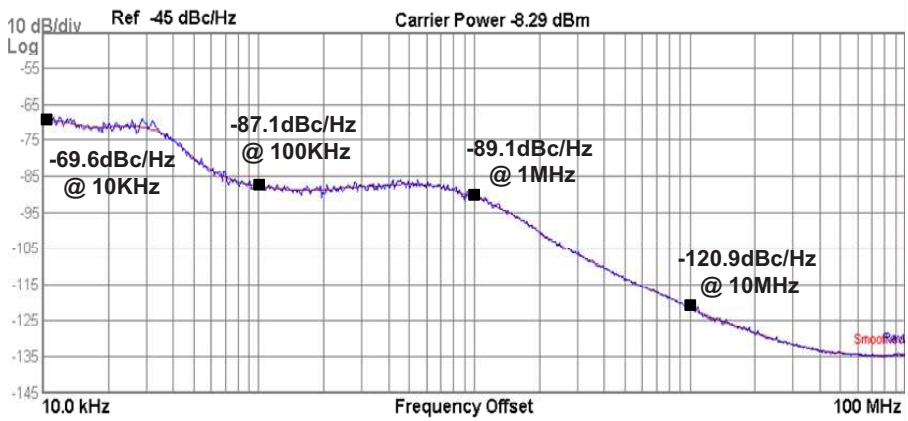
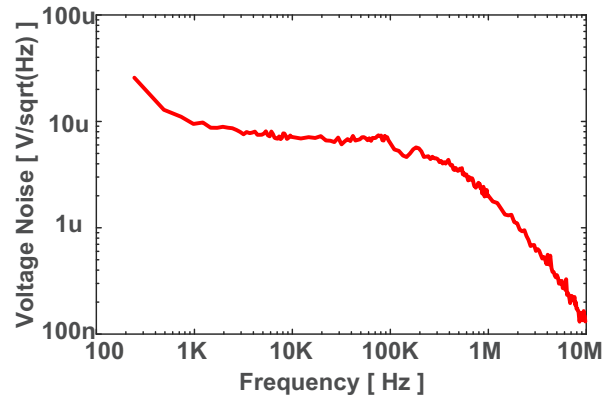
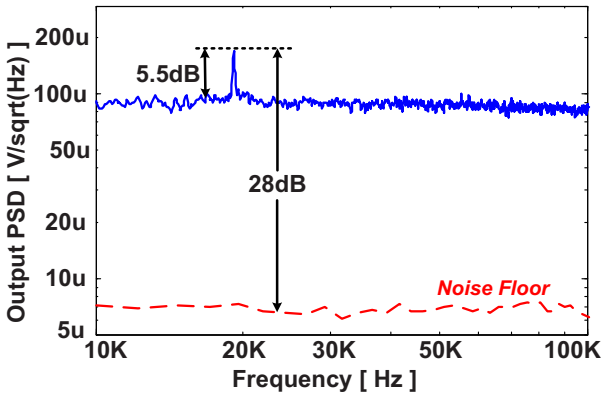


Figure 3.28: The measured phase noise of the divided LO signal in the receiver.

output signal in frequency and time domain, respectively. Fig. 3.28 shows the measured phase noise of the CML output signal in the receiver PLL (test point in Fig. 3.11). Since it is the LO signal divided by 32, the phase noise of the LO is 30 dB higher. At large offset frequency (> 1 MHz), the LO has similar phase noise compared to the transmitter. However, at lower offset frequency (< 100 KHz), the LO shows worse phase noise performance, which is caused by the inferior flicker noise of the reference clock used in the receiver. Using a signal analyzer, the output voltage noise spectrum density of one detector cell is measured with the transmitter chip turned off. As shown in Fig. 3.29(a). The noise density from 10 kHz to 100 kHz is almost flat with a value of around 6.8 $\mu V/\sqrt{Hz}$. Beyond 200 kHz, the noise starts to get filtered out by the baseband filter. With a 15cm transmitter-to-receiver distance, the measured output signal PSD is shown in Fig. 3.29(b). Since the phase noise of both RF and LO will be transferred to the output after mixing, the close-in phase noise of the output is limited. As a result, the signal power is spread within the 90 kHz bandwidth. However, due to the high sensitivity of the detector cells, the output still has a peak 28 dB higher than the noise floor. To get better use of the output signal



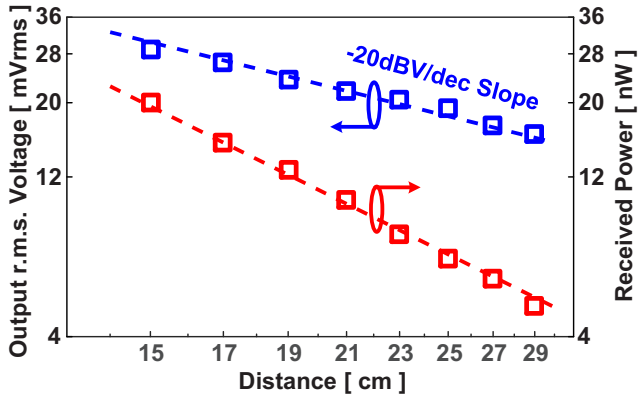
(a)



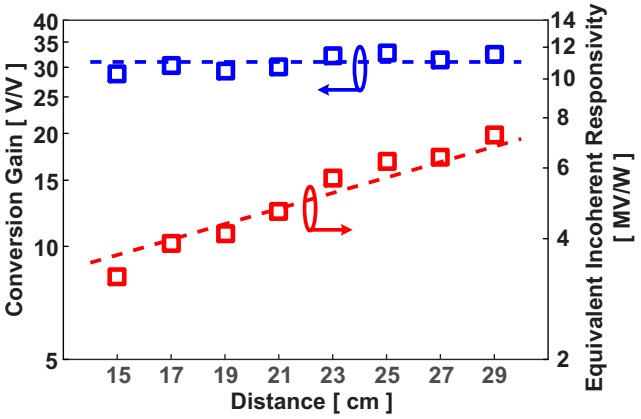
(b)

Figure 3.29: The measured receiver chip (a) output voltage noise spectrum density and (b) output signal power spectral density.

power, it is integrated from 10 kHz to 100 kHz to get an output rms voltage. The output rms voltage as well as the detector cell received RF power at different distances is shown in Fig. 3.30(a). A -20 dBV/dec slope is observed for the output rms voltage, which matches the theory of heterodyne detection and is different from the -40 dBV/dec slope observed in conventional incoherent detectors [52]. This is one of the factors which give rise to much higher sensitivity for the heterodyne detectors. There are two ways to obtain the detector cell received RF power. The first method is to use the setup in Fig. 3.21(b) to measure the power density at a certain distance and then calculate the power P_r



(a)



(b)

Figure 3.30: The measured receiver (a) output rms voltage as well as the received RF power at different transmitter-to-receiver distances and (b) conversion gain as well as equivalent incoherent responsivity at different transmitter-to-receiver distances.

a detector cell could receive if the receiver chip is positioned there:

$$P_r = \frac{P_{cal.}}{A_{horn}L}A_{rx} = \frac{P_{cal.}}{G_{horn}L}G_{rx} \tag{3.3}$$

where $P_{cal.}$ is the measured power with the calorimeter, A_{horn} and G_{horn} are the aperture size and gain of the horn antenna used, L is the loss of the additional WR-10 section and WR-10-3.4 taper, A_{rx} and G_{rx} are the aperture size and gain of the receiver on-chip patch antenna. The second way is to use Friis equation

to calculate the RF power one detector cell can receive:

$$P_r = \frac{P_{out,tx} D_{tx}}{4\pi d^2} A_{patch} = (\frac{\lambda}{4\pi d})^2 P_{out,tx} D_{tx} G_{rx} \tag{3.4}$$

where $P_{out,tx}$ and D_{tx} are the output power and directivity of the transmitter, d is the transmitter-to-receiver distance, G_{rx} is the gain of the receiver antenna. In our measurement, we adopted the first method and verified the results with the second method. The results are consistent with only minor differences. Assuming a 50-Ω impedance for the RF signal, a conversion gain from the received RF rms voltage to output rms voltage can be calculated using:

$$G_v = \frac{V_{rms}}{\sqrt{P_r \cdot 50\Omega}} \tag{3.5}$$

where V_{rms} is the output rms voltage and P_r is the received RF power. The conversion gain at different distances is shown in Fig. 3.30(b). The averaged conversion gain is 31.0 V/V. To compare with incoherent detectors, an equivalent incoherent responsivity is defined as the responsivity that an incoherent detector needs to generate the same output rms voltage with the same received RF power. This equivalent responsivity can be derived with [52]:

$$\Re_v = \frac{\pi V_{rms}}{\sqrt{2} P_r} \tag{3.6}$$

The receiver equivalent responsivity at different distances is also shown in Fig. 3.30(b). It is observed that, as the received power decreases, the receiver equivalent incoherent responsivity increases. This also reflects the effectiveness of enhancing detection sensitivity by using heterodyne detection. To make a fair comparison between coherent and incoherent imagers, a sensitivity is defined as the received RF power for the output signal to have SNR=1 within a 1-kHz bandwidth (corresponding to 1 ms time constant for fast imaging). The sensitivity of the proposed receiver is calculated to be 70.1 pW, which is around 10

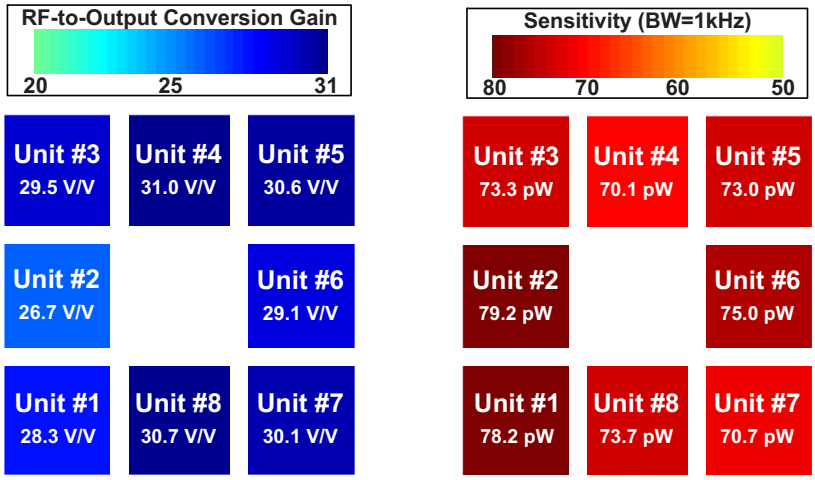


Figure 3.31: Performances of all the 8 detector cells: (a) conversion gain and (b) sensitivity under 1 kHz bandwidth.

times better compared to other state-of-the-art silicon detectors (as shown in Table 3.3). The sensitivity enhances even further with a larger bandwidth (about 20 times for 10 kHz bandwidth and 70 times for 100 kHz bandwidth) corresponding to faster imaging. The measured conversion gain and sensitivity for all the 8 detector cells are shown in Fig. 3.31. Thanks to the highly-symmetrical LO distribution network, the performances of the detector cells are quite uniform.

3.5.3 The Imager Demonstration

To put the transceiver into real use, a transmission mode terahertz imager is built up as shown in Fig. 3.32, which is composed of the transceiver chips, four Teflon lenses and a mechanical stepper. The first two Teflon lenses are used to focus the terahertz beam generated by the transmitter chip and form a focal plane. The two Teflon lenses on the receiver side are used to re-focus the

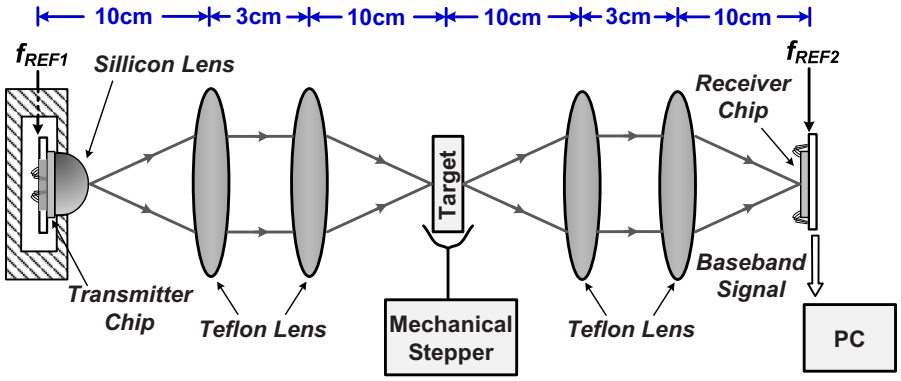


Figure 3.32: The imager setup using the proposed transmitter and receiver chips.

transmitted beam in order to increase the power that could be received by the receiver chip. The mechanical stepper is used to move the object on the focal plane for scanning.

With this imager, a few terahertz images are formed. Fig. 3.32 shows the THz image of a human tooth. Fig. 3.34 shows the image of a floppy disk, which provides information about the inside structure of the floppy disk. Fig. 3.35 shows the image of a student ID card with a metallic "UNIC" symbol attached to it. Beside the metallic "UNIC" symbol, the chip as well as the wire antenna inside the card is now visible.

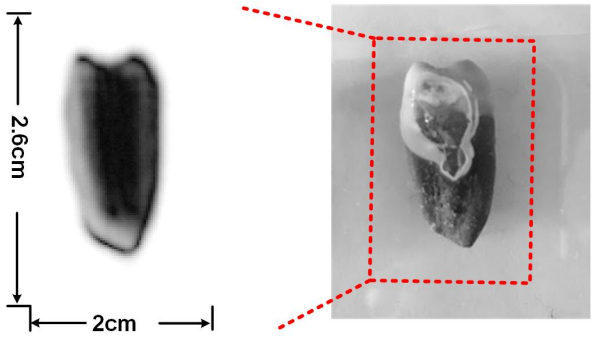


Figure 3.33: Image formed by the coherent imager: a human tooth (130×80 pixels).

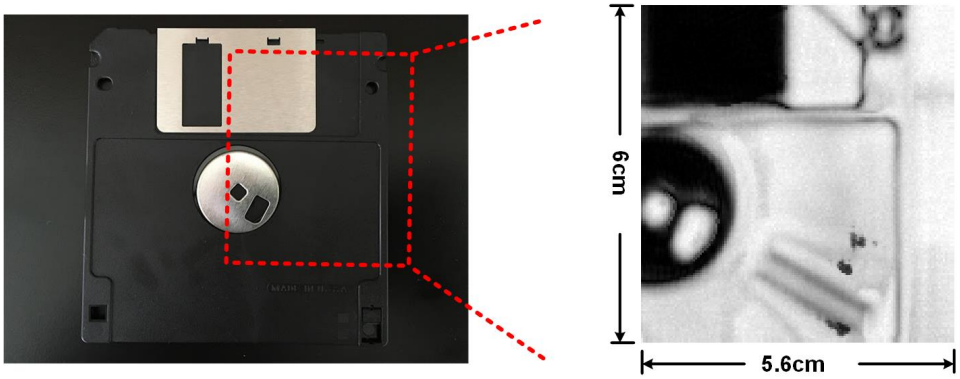


Figure 3.34: Image formed by the coherent imager: a floppy disk (150×140 pixels).

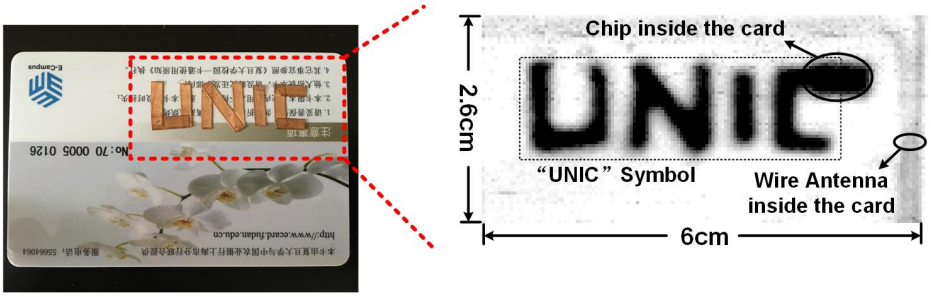


Figure 3.35: Image formed by the coherent imager: a student ID card with a metallic "UNIC" symbol attached to it (150×66 pixels).

3.6 Conclusion

Performance of the proposed transmitter and receiver chip is summarized in Table 3.1 and Table 3.2. The transmitter chip achieves a peak radiated power of 2 mW and a peak EIRP of 21.1 dBm with a total dc power consumption of 605 mW. The receiver chip achieves an equivalent incoherent responsivity of more than 7.26 MV/W and a sensitivity of 70.1 pW under an integration bandwidth of 1 kHz. The total dc power consumption of the receiver chip is 117 mW. A comparison with other terahertz imagers is given in Table 3.3. It can be seen that under the 1-kHz integration bandwidth, the proposed coherent imager can

achieve around 10 times better sensitivity compared to other state-of-the-art incoherent ones. The sensitivity enhances even further with a larger bandwidth (about 20 times for 10 kHz bandwidth and 70 times for 100 kHz bandwidth) corresponding to faster imaging. Using the PLL based architecture, no off-chip high-frequency high-power sources are needed. To our best knowledge, this work demonstrates the first fully-integrated coherent terahertz imaging transmitter and receiver pair on silicon.

Table 3.1: Performance Summary of the Transmitter

Output Frequency Range	319.0 ~ 323.0 GHz
Peak Radiated Power	2 mW
EIRP	21.1 dBm
Directivity	18.0 dBi
Peak Radiator Efficiency	0.41 %
Phase Noise	-67.4 dBc/Hz @ 100KHz offset -66.8 dBc/Hz @ 1MHz offset -87.2 dBc/Hz @ 10MHz offset
Power Consumption	433 mW (Radiator Array) 172 mW (PLL)

Table 3.2: Performance Summary of the Receiver

LO Tuning Range	152.5 ~ 164.8 GHz
Antenna Gain	2.2 dB
Output Voltage Noise	6.7 $\mu V/Hz^{1/2}$ @ 100KHz
RF-to-Output Conversion Gain	31.0 V/V
Equivalent Incoherent Responsivity	> 7.26 MV/W
Sensitivity (1 kHz BW)	70.1 pW
Power Consumption	41.6 mW (Detector Array) 75.5 mW (PLL)

Table 3.3: Comparison with Previous State-of-the-Art Works

Reference	Frequency	Array Size	Responsivity	Sensitivity [6]	Coherent Sensing	Technology
JSSC 2013 [24]	0.28 THz	4×4	336 V/W [1]	917 pW [7]	No	0.13-µm CMOS
	0.86 THz	single pixel	273 V/W [1]	1.33 nW [7]		
JSSC 2012 [25]	0.86 THz	32×32	140 kV/W [2]	3.16 nW [7]	No	65-nm CMOS
JSSC 2013 [26]	0.32 THz	4×4	18 kV/W [3]	1.08 nW [7]	No	0.18-µm BiCMOS
TTST 2015 [48]	0.26 THz	4×4	2.6 MV/W [4]	250~279 pW [7]	No	0.13-µm BiCMOS
This Work	0.32 THz	8-cell array	> 7.26 MV/W [5]	70.1 pW [7]	Yes	0.13-µm BiCMOS

1. 24 dB on-chip amplifier gain is de-embeded. 2. On-chip readout circuit gain and 5 dB off-chip VGA gain included.
3. 22 dB amplifier/buffer gain included. 4. 33~57.5 dB VGA gain included.
5. The equivalent resonsivity of the coherent detector is defined as: the responsivity an incoherent detector needs to generate the same output r.m.s. voltage with the same received power level. 60 dB baseband gain included.
6. The sensitivity is defined as the input power level for the output signal to have SNR=1 within 1 kHz bandwidth.
7. Assume noise spectrum density is flat within the 1 kHz bandwidth.

CHAPTER 4

EFFICIENT SPATIAL-ORTHOGONAL ASK TRANSMITTER FOR ULTRAHIGH-SPEED SHORT-RANGE COMMUNICATION

The terahertz band can provide vast spectrum for ultra-fast communication. However, since signal generation and modulation is still very challenging, in order to better utilize the benefit brought by terahertz, design innovations from both circuit level and system level are needed. In this chapter, innovative design of an efficient spatial-orthogonal ASK transmitter is demonstrated.

4.1 Introduction

The demand for wireless communication throughput is expanding drastically, however, the spectrum resources is becoming more and more limited in conventional RF bands. On the other hand, vast unallocated spectrum exists in the THz range, which can provide ultra-wide bandwidth for high speed communication. Compared with broadcasting of conventional RF frequencies, the line-of-sight nature also provide better security. Integrating THz communication systems onto silicon is highly desired for smaller size and lower cost, however, many challenges exist. First of all, signal generation efficiency in this frequency range is still low and modulation circuits normally introduce large loss. The lack of good power amplifiers also limits the output power of a transmitter. On the receiver side, lack of high-performance low-noise amplifiers causes poor noise performances. Fortunately, due to the small wavelength, antenna arrays can be implemented on chip to significantly enhance the antenna gain to improve the link budget [21].

Recently, THz communication systems have been demonstrated on silicon. In [53], a 210-GHz fundamental-frequency transceiver is presented. Due to the limited performance of the power amplifier and the low-noise amplifier, the achieved baseband signal SNR is less than 14 dB. Several new topologies have also been introduced. In [27] and [28], 240-GHz 16-Gb/s QPSK transmitter and receiver are presented. In the transmitter, a multiplier-last architecture is used, in which signal generation and modulation happen at lower frequency and a frequency tripler pushes the output into terahertz band. However, only limited modulation schemes are supported using this scheme and the spectral efficiency is low. The tripler also introduces a large conversion loss. A 300-GHz 32-QAM transmitter is introduced in [54], which uses 6 frequency channels and a 17.5-Gb/s capacity is achieved in each channel. Cubic mixers are used to mix the second harmonic of the LO with the IF. Even though massive power combining is used to increase the output power, due to the large conversion loss of the cubic mixer, only -14.5 dBm output power is achieved while consuming 1.4 W dc power.

Most previous transmitter architectures in this frequency range rely on multiplier-based signal sources [27, 28, 54], which have relatively lower power efficiency [29]. Meanwhile, large power loss happens in the modulation path, which limits the transmitter output power, efficiency and communication range (1 cm is demonstrated in [27], wafer probing and waveguide are used in [54]). In the rest of this chapter, design of a novel spatial-orthogonal ASK (SO-ASK) transmitter architecture is demonstrated. In the transmitter, harmonic oscillators are used for signal generation instead of multiplier-based sources for better power efficiency and higher integration level [1]. A high-speed constant-load modulation switch is also proposed to provide high date rate while significantly

reduce the modulation loss. Transmitter array is implemented for better EIRP to achieve longer communication range. Using polarization diversity, the SO-ASK scheme doubles the throughput. Link capacity can be further improved with multi-level modulation. A 220-GHz transmitter prototype is fabricated in a 0.13-μm SiGe BiCMOS process, which achieves a 24.4 Gb/s total data rate over a 10-cm range. With an external Teflon lens system, the range is further extended to 52 cm. This prototype also shows much higher transmitter efficiency compared with prior art according to our measurement.

4.2 Principle and Analysis of the Proposed Spatial-Orthogonal ASK Transmitter Architecture

Generation of THz power on silicon is relatively inefficient, consequently, it is desired to make full use of the generated power. In this design, we seek to maximize the signal generation efficiency while minimize the loss in the modulation. Besides, compact design is desired to facilitate array configuration for higher EIRP and better link budget.

4.2.1 Principle of the Spatial-Orthogonal ASK Transmitter

In this frequency range, signal modulation can be very lossy. For example, in [27], with 5 dBm LO power, the 80-GHz QPSK modulator can provide only -5 dBm output power. Adding the ~12-dB conversion loss of the final stage 240-GHz tripper, significant loss is associated with the modulation. For the cubic mixer in [54], with 5 dBm LO power at 97 GHz, the 300-GHz output power is

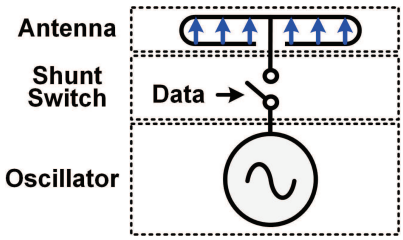


Figure 4.1: The oscillator-based OOK transmitter cell structure.

below -15 dB. For better transmitter performance, minimizing the modulation loss is critical. Shown in Fig. 4.1 is an oscillator-based OOK transmitter. Compared with multiplier-based signal sources that are widely used in previous architectures, oscillators are more power efficient [29]. It is also self-sustaining, which means no high-frequency drive signal is needed and higher integration level can be achieved [1]. It will be shown in Section 4.3 that, with the proposed high-speed constant-load modulation switch, the power utilization ratio (difference of the percentage of power reaches the antenna port between switch "on" and "off") achieved is more than 60%. This corresponds to a modulation loss of only ~2 dB, which means the signal power generated by the oscillator is well utilized and much higher RF output power can be generated. The structure is also very compact, which facilitates the array configuration. However, there are two obvious drawbacks: (i) the incoherent operation causes lower receiver sensitivity and (ii) the simple modulation scheme provides limited spectral efficiency. Details about the first drawback will be discussed in the next section. To compensate the second drawback, polarization diversity can be utilized. It has been shown that two orthogonal polarization states of planar waves can support two separate information channels [55]. As shown in Fig. 4.2, two transmitter cells with linearly-polarized antennas are placed perpendicular to each other. With the two spatial orthogonal channels, the capacity is doubled. If the information

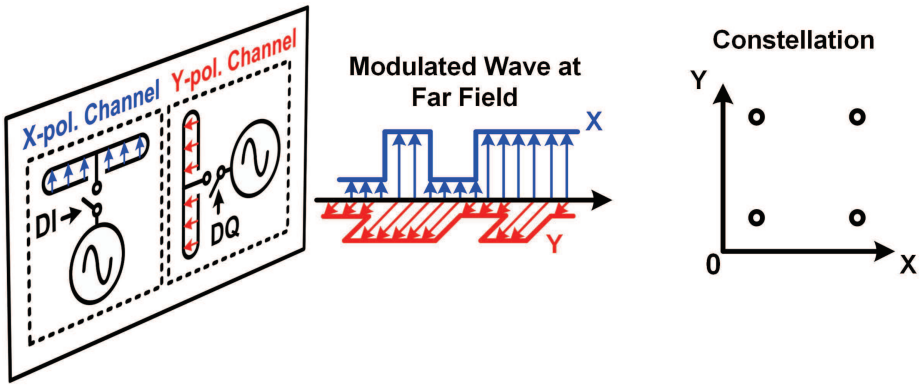


Figure 4.2: Principle of the spatial-orthogonal ASK modulation based on polarization diversity and the equivalent constellation plot.

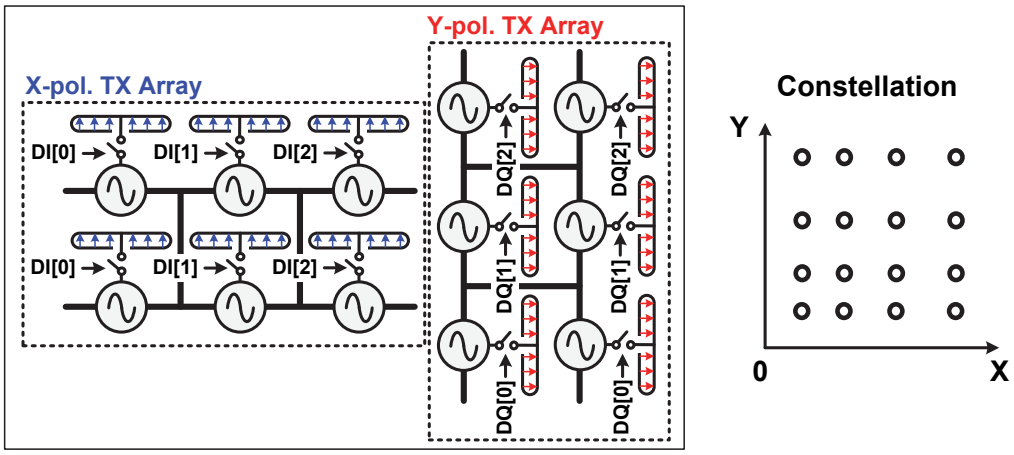


Figure 4.3: Principle of the 4-level spatial-orthogonal ASK transmitter with 2×3 array configuration inside each channel as well as the equivalent constellation plot.

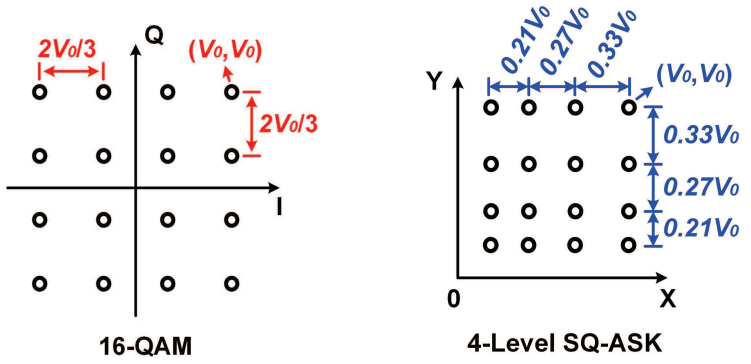
in the X- and Y-polarized channels is combined, the constellation plot in Fig. 4.2 is formed. To further increase the spectral efficiency and capacity, multi-level ASK modulation can be implemented inside each spatial channel. As shown in Fig. 4.3, the transmitter has a 2×3 array in each channel. With thermometer coding for DI[0:2] and DQ[0:2], a 4-level SO-ASK modulation is realized with constellation plot shown in Fig. 4.3. This scheme further doubles the capacity. Besides, with power combining and higher antenna gain obtained with the

array, larger transmitter EIRP is achieved. In summary, this transmitter architecture can achieve high power, excellent power efficiency as well as good data rate with simpler implementation and smaller chip area.

4.2.2 Link Budget Analysis and Comparison

The proposed SO-ASK transmitter architecture can significantly reduce the modulation loss, hence achieving higher output power and EIRP. However, as mentioned previously, the incoherent operation requires higher transmitter power to compensate the lower receiver sensitivity in order to maintain the same system performance. Fortunately, the disadvantage of incoherent operation becomes much less significant in communication systems due to the high SNR requirement as well as the high noise floor caused by the large bandwidth. On the other hand, higher transmitter EIRP benefited from the lower modulation loss and easier array configuration due to the simpler and more compact structure can significantly improve the system link budget. To show this point more clearly, a comprehensive system performance comparison between a typical 16-QAM and the proposed 4-level SO-ASK modulation scheme is performed.

Shown in Fig. 4.4 are the constellation plots of the typical 16-QAM and the 4-level SO-ASK. Due to the directivity of the antenna array slightly changes with turning on different numbers of transmitter cells, the constellation of the 4-level SO-ASK has a little distortion. Fig. 4.4(b) is drawn according to simulation. Based on the constellations, theoretical calculation and MATLAB simulation of bit error rates (BER) under different SNRs are performed for both cases, with



(a) (b)

Figure 4.4: Constellation plots of (a) the typical 16-QAM and (b) the proposed 4-level spatial-orthogonal ASK.

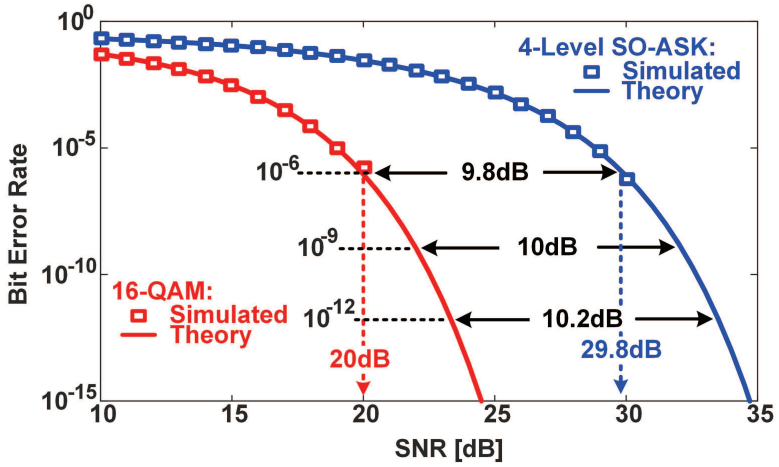
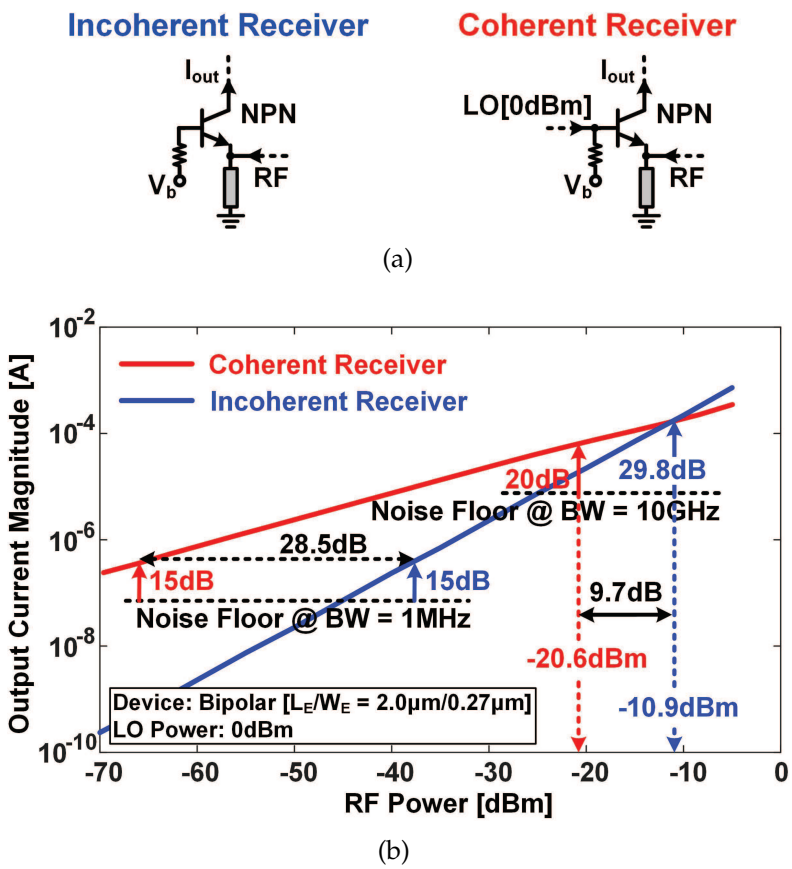


Figure 4.5: Bit error rate analysis of the 16-QAM and the proposed 4-level spatial-orthogonal ASK.

results shown in Fig. 4.5. The results are obtained with the following assumptions: (i) AWGN channel model [56]; (ii) Grey code [57] is used in bit mapping in both schemes and (iii) all the symbols have equal probability. It shows that, for a reasonable BER range ($< 10^{-6}$), the proposed SO-ASK scheme needs around 10 dB higher SNR to achieve the same BER. This inferior performance stems from the crowded and slightly distorted constellation in Fig. 4.4(b). For a target BER of 10^{-6}, the minimum SNR required for both cases are 20 dB and 29.8 dB,



(a)

(b)

Figure 4.6: Receiver sensitivity analysis of the coherent 16-QAM system and the proposed incoherent 4-level spatial-orthogonal ASK system: (a) bipolar transistor configured as both coherent and incoherent receiver front end and (b) sensitivity simulation results.

respectively.

To find out how this disadvantage will affect the receiver sensitivity, circuit level simulations are performed. The same bipolar transistor from the STMicroelectronics 0.13-μm SiGe BiCMOS technology with emitter length and width of 2.0 μm and 0.27 μm, respectively, is used to configure the receiver front end for both modulation schemes, as shown in Fig. 4.6(a). The simulation is performed at an RF frequency of 220 GHz. For the SO-ASK, an incoherent power detector is enough. For the 16-QAM, the transistor is configured into a mixer

with RF power injected from the emitter and a 220.1-GHz LO with 0 dBm power pumped into the base. The simulated output current magnitude with different input RF power is shown in Fig. 4.6(b). The noise floor is the rms current noise derived by integrating the output collector noise current inside the assumed bandwidth. In narrow-band applications such as imaging and spectroscopy, coherent sensing significantly enhances the receiver sensitivity [4, 17]. As shown in Fig. 4.6(b), with 1 MHz bandwidth and minimum SNR of 15 dB, the sensitivity difference between the coherent and incoherent receiver is almost 30 dB. However, in communication systems, large bandwidth is normally required, which significantly reduces this sensitivity difference: with bandwidth of 10 GHz and targeted BER of 10^{-6} (corresponding to minimum SNR of 20 dB and 29.8 dB for the two cases), the sensitivity difference is only 9.7 dB. This difference will further shrink if larger bandwidth is required for higher capacity or higher SNR is required for better BER. It is noteworthy that, in the previous comparison, we assume fundamental LO is applied, however, in real scenario, fundamental LO with high power is hard to obtain and subharmonic mixing is often used [4, 54]. In this case, the sensitivity difference will also significantly shrink. As discussed previously, in the SO-ASK transmitter, the switch-based ASK modulation can achieve much lower modulation loss (10 dB or more), which can compensate the sensitivity disadvantage caused by incoherent operation. It is mentioned previously that, array configuration can effectively increase the transmitter EIRP and benefit the link budget. There are two ways to configure the array: (i) replicate just the antenna and use the transmitter to feed the antenna array; (ii) replicate the whole transmitter cell to form a transmitter array. In theory, with an array size of N, transmitter array can produce N^2 larger EIRP while antenna array only improves the EIRP by N. For previous transmit-

ter architectures, there are two obstacles for implementing transmitter array: (i) the high frequency LO distribution with acceptable delay/phase mismatch is complicated to achieve; (ii) the large physical size limits the smallest antenna distance and grating lobes may degrade the EIRP enhancement. Even for implementing antenna array, RF signal distribution and impedance matching can be complicated and lossy when array size is large. However, with much more compact size and no need for LO distribution, the proposed SO-ASK system is very convenient to be replicated to form large transmitter arrays. Besides, for the SO-ASK system, only incoherent receiver is required. Again, with compact size and no issue of LO distribution, incoherent receivers are also much easier to form arrays to increase the receiver antenna directivity and further enhance the system performance. It is worth mentioning that, even though there are many other devices and topologies for implementing coherent and incoherent receivers, the results in Fig. 4.6(b) represents a typical trend. Intuitively, coherent systems can offer higher sensitivity due to LO power is normally much higher than the received RF power. However, in THz communication systems, with larger input power requirement caused by larger bandwidth and higher minimum SNR, the difference between RF and LO power shrinks, so does the sensitivity difference. Consequently, the qualitative conclusions drawn here are true for not only the implementation shown in Fig. 4.6(a) but also for most other similar cases.

In summary, the proposed SO-ASK transmitter has the potential to achieve better system link budget (meaning higher signal quality or longer communication range) as well as similar data rate and spectral efficiency with lower system complexity, smaller area and higher power efficiency. Also, with compact size and no need for high frequency LO distribution, it is highly scalable into larger

arrays, which can help achieving longer communication range or more levels of modulation for even higher data rate.

4.3 Design of the 220-GHz Spatial-Orthogonal ASK Transmitter Prototype

The proposed 4-level SO-ASK transmitter has two perpendicular 2×3 transmitter arrays as shown in Fig. 4.3. Each transmitter cell is composed of a harmonic oscillator, a compact slot antenna and a constant-load high-speed modulation switch. Next, design details of the circuit blocks are described.

4.3.1 The Slot Antenna

To create spatial-orthogonal channels, the antenna needs to be linearly polarized. For a high data rate, a wide antenna bandwidth is required. A compact design is also desired for easier array configuration and lower cost. In this work, a slot antenna shown in Fig. 4.7 is adopted. The antenna length is 300 μm, which is around half wavelength at 220 GHz. The width is tuned to 20 μm

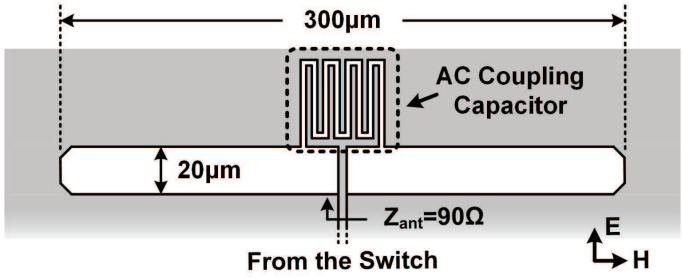
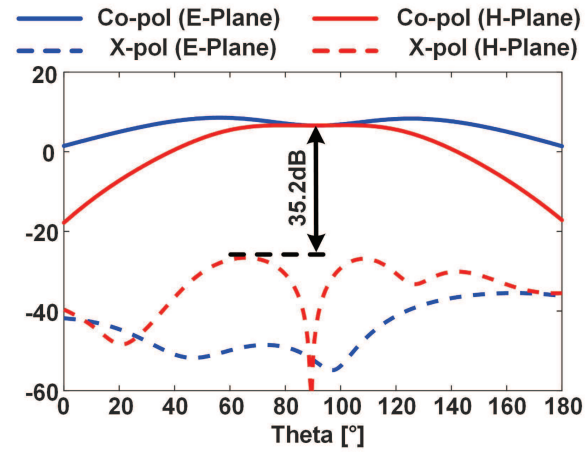
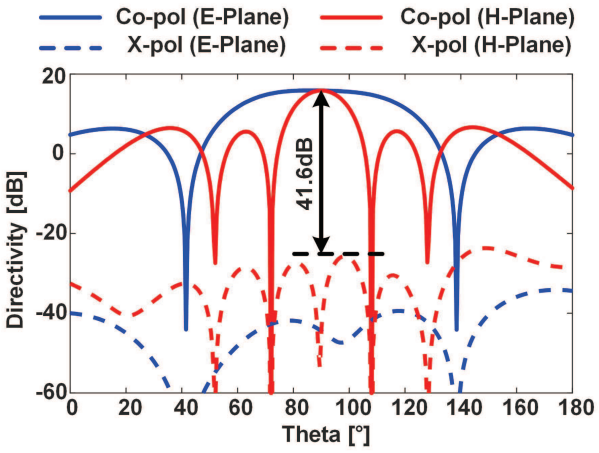


Figure 4.7: The 220-GHz compact slot antenna.



(a)



(b)

Figure 4.8: Simulated antenna directivity of the (a) slot antenna and the (b) 2×3 array.

for a suitable input impedance. A custom-designed AC-coupling capacitor is used to separate the dc of the antenna input port from the ground. According to HFSS simulation, bandwidth of the antenna is more than 30% (~68 GHz near 220 GHz), which is wide enough for the transmitter. The antenna input impedance and efficiency is 90 Ω and 63%, respectively. It also has a small size, which is suitable for array configuration. The simulated radiation patterns of the slot antenna and a 2×3 array formed with this antenna are shown in Fig. 4.8.

For the array, a broadsided directivity is simulated to be 15.9 dBi and the cross-polarization is more than 40 dB lower than the co-polarization, which ensures very good isolation between the two spatial-orthogonal channels.

4.3.2 The Harmonic Oscillator

The oscillator is the most power hungry part in the transmitter, hence, its generated power and efficiency is of great importance. For array configuration, a compact design is also desired. Since the targeted frequency 220 GHz is close to the device f_{max} in this process (f_{max} = 280 GHz [50]), harmonic oscillator is used. For optimal output power, harmonic generation efficiency as well as compact size, the return-path gap coupler (RPGC) based self-feeding oscillator structure is used. Detailed working principle and design of this oscillator structure have been introduced in Chapter 2. The self-feeding structure can provide the transistors with optimum collector-to-base phase shift for optimal harmonic gen-

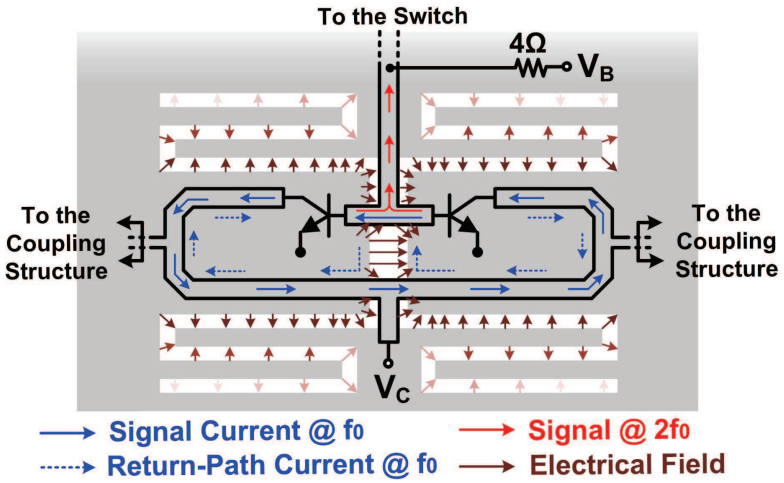
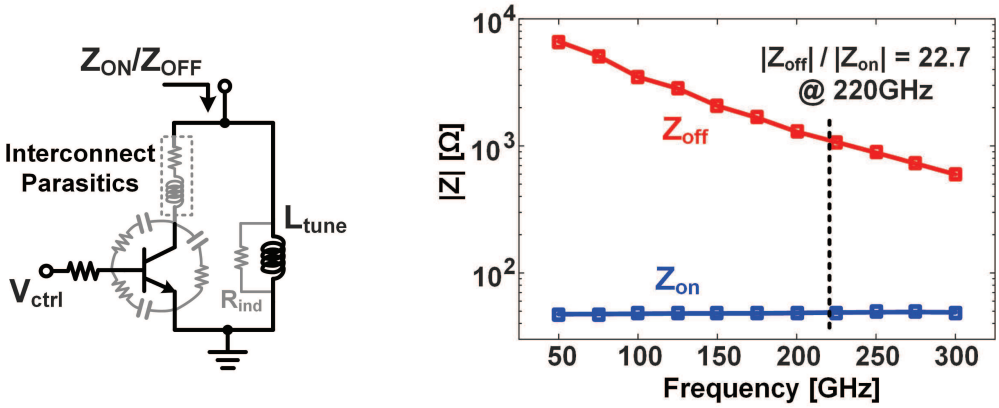


Figure 4.9: Schematic of the return-path gap based self-feeding harmonic oscillator.

eration; the RPGC structure can provide the desired collector-base isolation at the second harmonic to eliminate the self-power-cancellation/loading effect; the RPGC structure also naturally separates the dc of the transistors' base and collector for optimal biasing. The generated second harmonic power is sent to the switch for modulation. Two additional ports at the two sides of the self-feeding lines are for synchronization with neighboring oscillators in the transmitter array. According to simulation, under a supply voltage of 2 V and bias current of 15 mA for each transistor, the optimum load of the oscillator is 14 Ω, and each of the oscillator can generate 1.4 mW power at 220 GHz with a dc-to-terahertz efficiency of 2.5%. In principle, frequency tuning is not important in this system, however, it is worth mentioning that, based on parasitic tuning [1], the oscillator can achieve a total tuning range of around 10%.

4.3.3 The Constant-Load High-Speed Modulation Switch

Designing a high-performance switch at this frequency with ultra-fast switching speed, low insertion loss and good isolation when turned off is challenging. In this design, shunt switch topology is used for its low insertion loss. Shown in Fig. 4.10(a) is a bipolar transistor used as a shunt switch. With the parasitic capacitance tuned out with the shunt inductor L_{tune} , the impedance seen from the collector node is near pure resistive both when the transistor is "on" and "off". With ideal shunt inductor L_{tune} , the simulated "on" and "off" impedance of the transistor Z_{on} and Z_{off} are shown in Fig. 4.10(b). As we can see, Z_{on} remains relatively constant while Z_{off} drops quickly with frequency. This is caused by the quality factor of the parasitic capacitances of the transistor decreases with frequency, which causes a higher leakage of signal from the transistor collector



(a) (b)

Figure 4.10: The shunt switch based on a bipolar transistor: (a) schematic and (b) simulated "on" and "off" switch impedances at different frequencies (assume ideal L_{tune}).

to the emitter, thus smaller Z_{off}. At 220 GHz, the on/off ratio of the shunt switch $|Z_{off}/Z_{on}|$ is 22.7. It is worth mentioning that, in reality, due to the limited quality of passive on-chip components, the parallel parasitic resistance of L_{tune} [R_{ind} in Fig. 4.10(a)] degrades the switch on/off ratio to $|(Z_{off} + R_{ind})/(Z_{on} + R_{ind})|$. At 220 GHz, with L_{tune} implemented with G-CPW transmission line, the simulated on/off ratio drops to around 10.

For ultra-fast switching, the switch needs to have a constant input impedance so that the oscillator is not disturbed and there is no need to wait for it to settle until the next switching. In this design, a constant-load shunt switch is proposed. As shown in Fig. 4.11(a), the switch is composed of two shunt bipolar switches and a quarter-wave length transmission line. When both switches are "on" or "off", the switch input impedance $Z_{sw,on}$ and $Z_{sw,off}$ are,

$$Z_{sw,on} = \frac{Z_{on1}Z_0^2}{Z_0^2 + Z_{on1}Z_{on2}}, \quad Z_{sw,off} = \frac{Z_{off1}Z_0^2}{Z_0^2 + Z_{off1}Z_{off2}} \tag{4.1}$$

in which, Z_{on1}, Z_{off1}, Z_{on2} and Z_{off2} are the "on" and "off" impedances of the two bipolar shunt switches, Z_0 is the characteristic impedance of the quarter-wave

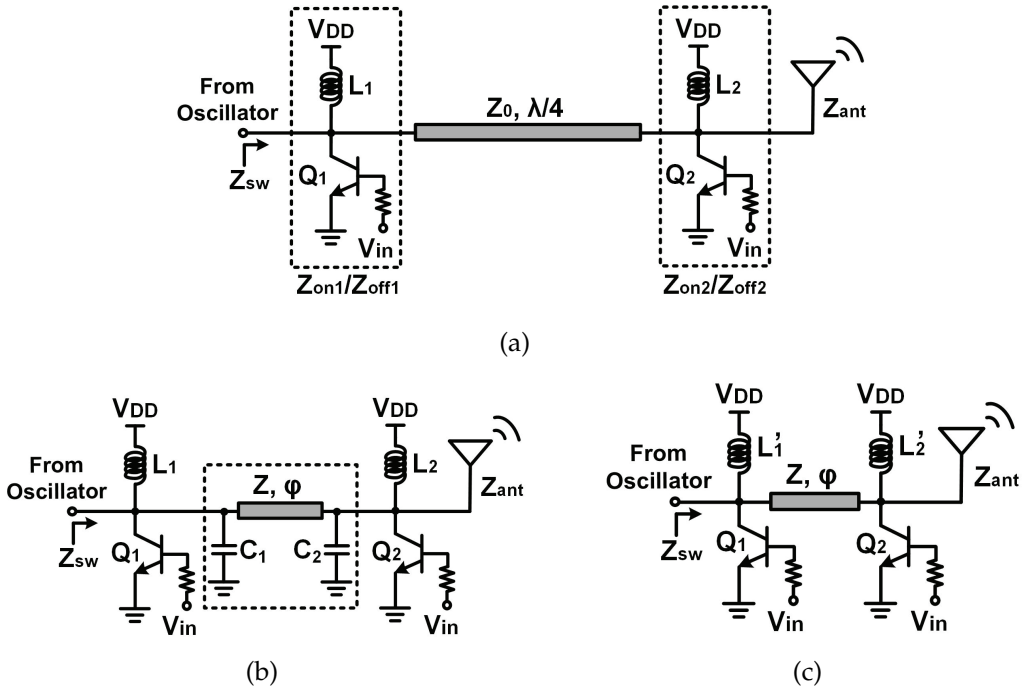


Figure 4.11: Evolving of the constant-load high-speed modulation switch: (a) the initial form, (b) after size shrinking and (c) after tuning out of the capacitors.

line. In order to have the switch input impedance remain constant near the optimum load of the oscillator (Z_{opt} = 14Ω), the following equation needs to be satisfied,

$$\frac{Z_{on1}Z_0^2}{Z_0^2 + Z_{on1}Z_{on2}} = \frac{Z_{off1}Z_0^2}{Z_0^2 + Z_{off1}Z_{off2}} = Z_{opt} \tag{4.2}$$

If on/off ratios of both switches are assumed to be 10, given a Z_{on1} , with (4.2), all other parameters can be calculated. The power utilization ratio is defined as the difference of percentage of power sent to the antenna when the switch is "on" and "off". With different Z_{on1} , power utilization ratio of the switch is simulated as shown in Fig. 4.12. For optimal power utilization ratio and room for process variation, Z_{on1} is chosen to be 21 Ω.

It has been mentioned previously, compact design is preferred for array configuration. In the switch structure shown in Fig. 4.11(a), the quarter-wave line

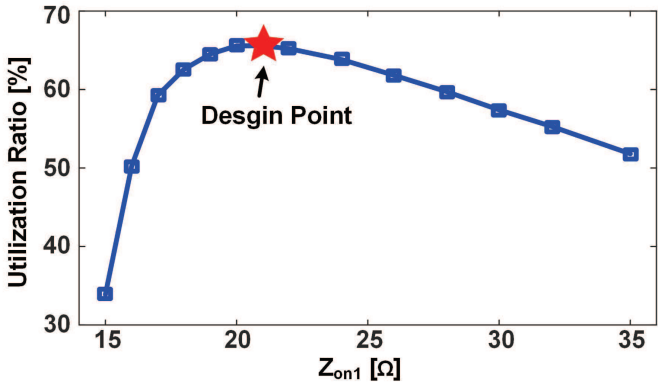


Figure 4.12: The simulated terahertz power utilization ratio vs. Z_{on1}. The design point is chosen near the peak of the curve.

takes large area. To reduce the size, as shown in Fig. 4.11(b), the quarter-wave line can be replaced with a much shorter line section and two lumped capacitors [59], with:

$$Z = Z_0/sin\varphi \tag{4.3}$$

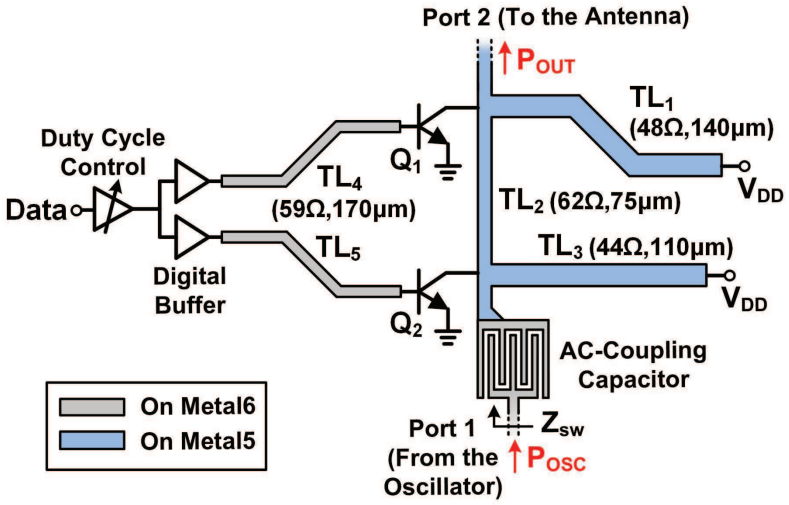
$$\omega C_1 = \omega C_2 = (1/Z_0)cos\varphi \tag{4.4}$$

where Z and φ are the impedance and electrical length of the transmission line section, C_1 and C_2 are the values of the two lumped capacitors. Capacitor C_1 and C_2 can then be tuned out with part of L_1 and L_2 as shown in Fig. 4.11(c). The new inductors $L_1^{'}$ and $L_2^{'}$ can be calculated as:

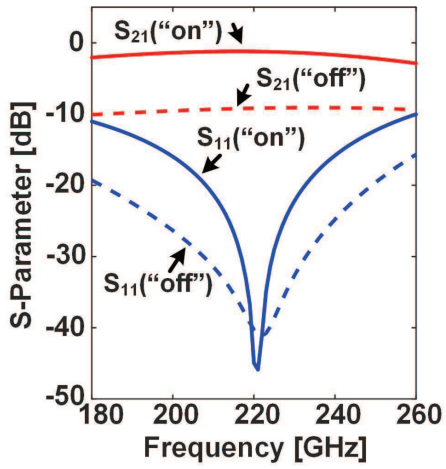
$$\omega L_1^{'} = \omega L_1 - \frac{1}{\omega C_1} \tag{4.5}$$

$$\omega L_2^{'} = \omega L_2 - \frac{1}{\omega C_2} \tag{4.6}$$

Comparing the switch in Fig. 4.11(c) and Fig. 4.11(a), beside the smaller size of the quarter-wave length line, there is an additional benefit. According to equation (4.5) and (4.6), the inductors $L_1^{'}$ and $L_2^{'}$ are smaller than L_1 and L_2. Since the quality factor of passive components with similar implementation do not change much at a certain frequency, the parallel parasitic resistance [R_{ind}



(a)



(b)

Figure 4.13: Final design of the constant-load high-speed modulation switch: (a) schematic and (b) S-parameter simulation.

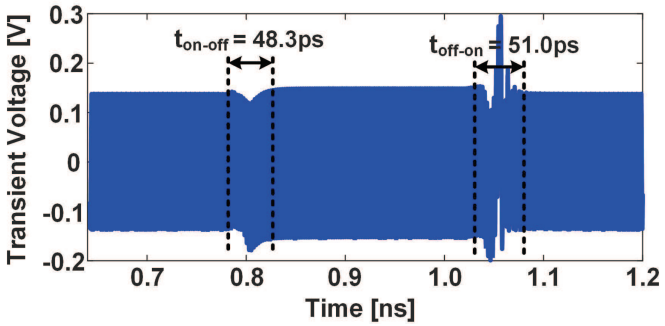
in Fig. 4.10(a)] of $L_1^{'}$ and $L_2^{'}$ is larger, which means a better switch on/off ratio. This, along with lower passive loss due to shorter lines, helps to achieve a higher power utilization ratio.

Final structure of the constant-load high-speed shunt switch is shown in Fig. 4.13(a). The lossy Via connections from the transistors to transmission lines will lower the switch on/off ratio and increase the insertion loss. To alleviate this

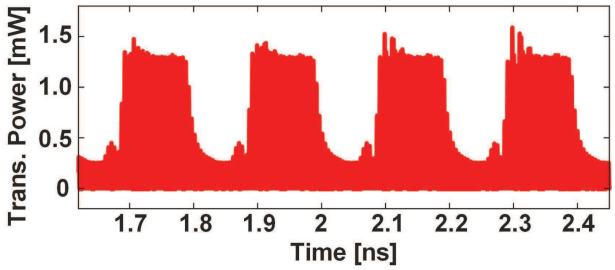
Table 4.1: Static Simulation Results of the Constant-Load Switch with 90 Ω Antenna Load at 220 GHz

	Z_{off}/Z_{on}
Switch 'Q1'	9.7
Switch 'Q2'	9.4

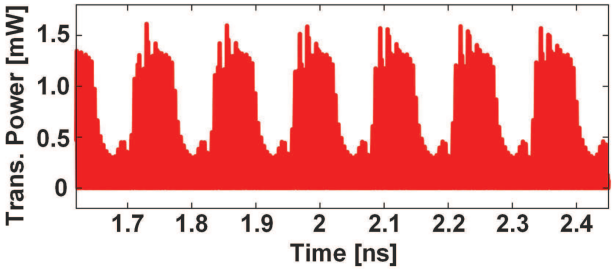
Data	"1"	"0"
Z_{sw}	(14.1 + j0.2) Ω	14.0 Ω
P_{OUT}/P_{OSC}	12.1%	75.6%



(a)



(b)



(c)

Figure 4.14: Dynamic simulation results of the constant-load high-speed modulation switch: (a) the oscillator output waveform while switching, as well as transient power at the output of the switch with input clock rate of (b) 5 GHz and (c) 8 GHz.

impact, $TL_1 - TL_3$ are implemented on the second top metal, M5, instead of the top metal, M6 (M5 and M6 have the same thickness of 3 μm in this process). To reduce time constant for faster switching, biasing resistors in Fig. 4.11(c) are replaced with transmission lines TL_4 and TL_5. To maintain high impedance at the base of Q_1 and Q_2 for low switch insertion loss, TL_4 and TL_5 are near quarter-wave length to transform the low digital buffer output impedance into a high impedance. Size of the two digital buffers are chosen to minimize the input data delay mismatch between the two paths. A duty-cycle control is also implemented to shape the input waveform. The drawback of the size shrinking described previously is the reduction of the bandwidth. However, according to the S-parameter simulation results shown in Fig. 4.13(b), the achieved bandwidth is still more than 40 GHz, which is wide enough for the system. At frequency point of 220 GHz, the simulated switch performances are given in Table 4.1. The switch input impedance remains around 14 Ω during switching, and 63.5% of the input power is utilized. Fig. 4.14(a) shows the simulated transient oscillator output waveform while the switch toggles. Due to the input impedance of the shunt switch seen by the oscillator is not exactly constant, there will be a small disturbance of the oscillation during the switching. However, since the recover time is only about 50 ps, ultra-fast switching can still be achieved. Fig. 4.14(b) and Fig. 4.14(c) are the simulated transient power delivered to the antenna with 5 GHz and 8 GHz sinusoidal waves as data input, which show a switching speed higher than 8 GHz. This means the achievable data rate with the 4-level SO-ASK transmitter can exceed 64 Gb/s.

4.3.4 Coupling of the Transmitter Cells

To obtain higher EIRP and functionality of multi-level modulation, each spatial channel has a 2×3 transmitter array as shown in Fig. 4.3. Inside each array, all the oscillators need to be synchronized for coherent power combining. To achieve this, a coupling network shown in Fig. 4.15 is designed. To explain how the coupling network works, a simpler case with four oscillators shown in Fig. 4.16(a) is discussed. Relative to OSC_1, its neighbors OSC_2 and OSC_3 can be either in-phase or out-of-phase. Consequently, there are four primary modes, and combination of the four modes can form any arbitrary phase relation among them. In these modes, center points A and B in Fig. 4.16(a) present either virtual open or virtual ground, and the impedance seen by OSC_1 under each mode can be determined as shown in Table 4.2. The results are also plotted on a smith chart for more intuitive comparison as shown in Fig. 4.16(b). As we can see, in three of the four primary modes, oscillators see low impedances, which are equivalent to large capacitive or inductive loads, and the oscillation will be disturbed. This means the three modes are not well supported with the given

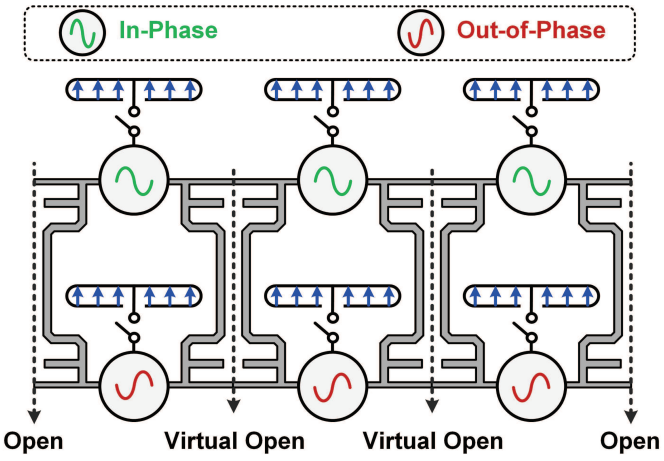


Figure 4.15: Coupling network among the 2×3 transmitter array.

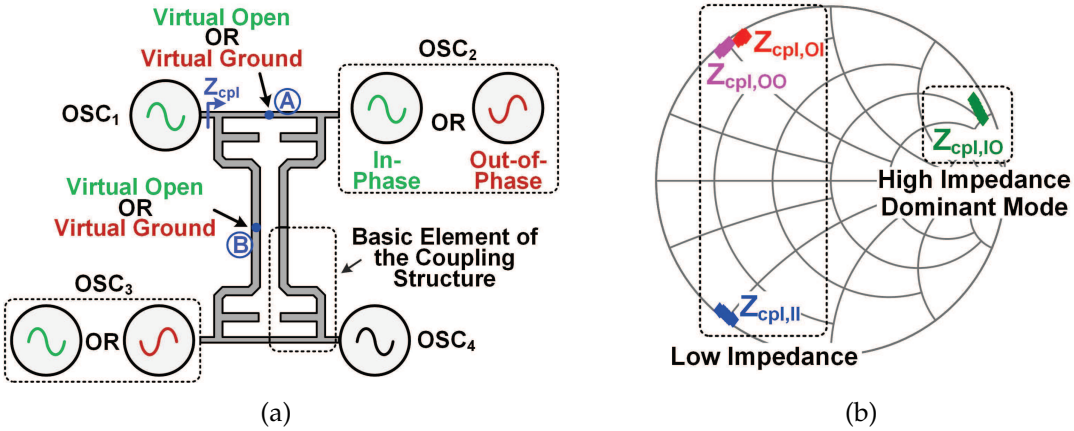


Figure 4.16: Analysis of the coupling network in the transmitter array: (a) four-oscillator case and (b) simulated impedances seen by the oscillators in the four modes.

Table 4.2: The Impedance of the Coupling Network Under Different Modes

OSC_2 \ OSC_3	In-Phase	Out-of-Phase
In-Phase	$Z_{cpl,II}$ (0.7 – j24.2) Ω	$Z_{cpl,IO}$ (36.1 + j230.0) Ω
Out-of-Phase	$Z_{cpl,OI}$ (0.7 + j23.6) Ω	$Z_{cpl,OO}$ (1.1 + j27.7) Ω

structure. Only when OSC_2 is in-phase and OSC_3 is out-of-phase, the oscillators see a large impedance and the oscillation is not affected, which makes it the dominant mode. For the same reason, in the 2×3 array shown in Fig. 4.15, the fundamental signals of the oscillators are in-phase within the upper row and the lower row in steady state, but between the two rows, they are out-of-phase. As a result, the central line of the two coupling structures among the transmitter cells present virtual open, as shown in Fig. 4.15. If the two sides of the whole array is left open, the symmetry of the whole array is well preserved. Since the oscillators in the array are either in-phase or out-of-phase with each other, their second harmonic will all be in-phase and power combining is obtained. Also, as men-

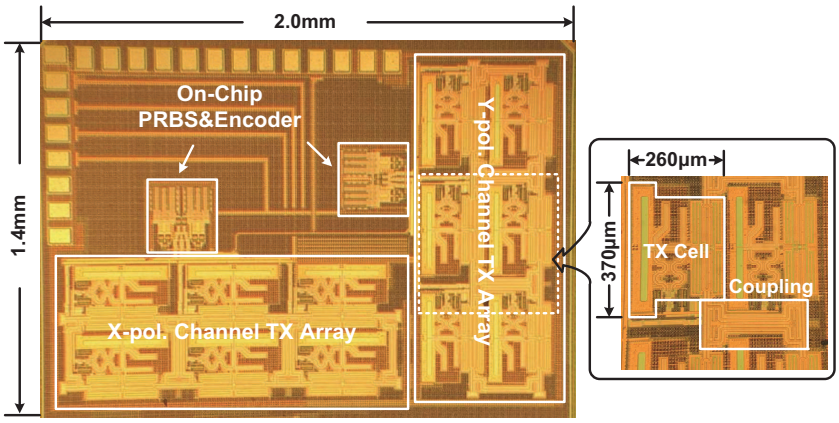
tioned before, the coupling network presents high impedance, consequently, it has almost no loading effect to the oscillators and little power is injected into the structure, which means negligible additional loss.

4.3.5 On-chip PRBS Generator and Encoder

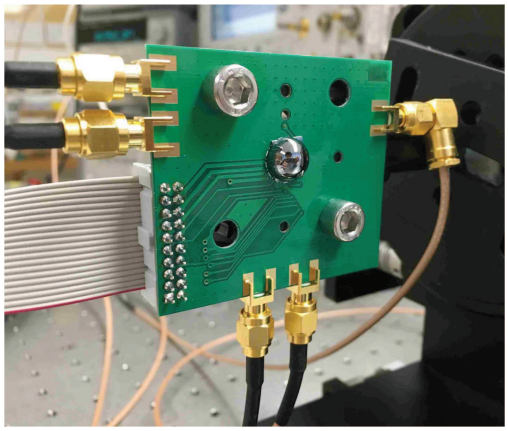
For ease of measurement, pseudo-random binary sequence generator (PRBS) and thermometer encoder are included in each spatial channel. With clock signal provided off-chip, the PRBS can generate two synchronized independent $(2^7 - 1)$ pseudo-random sequences. When multi-level function is turned on, the two sequences are fed into the thermometer encoder to provide inputs for the transmitter array. When multi-level is off, the thermometer encoder is bypassed, and one sequence is directly used as data input for the whole array.

4.4 Experimental Results

The prototype spatial-orthogonal ASK transmitter chip is fabricated using the STMicroelectronics 0.13-μm SiGe BiCMOS process with the chip and PCB photos shown in Fig. 4.17. With the ultra-compact design for all the blocks, the size of one transmitter cell is as small as 370 μm $\times$ 260 μm, which is the smallest wireless THz transmitter for communication application to our best knowledge (around 20 times smaller compared to [27] and 60 times smaller than [54]). In each spatial channel, the 2×3 transmitter array has an area of 1.3 mm $\times$ 0.6 mm. The whole chip dimension is 1.4 mm $\times$ 2.0 mm.



(a)



(b)

Figure 4.17: The transmitter prototype chip (a) die photo and (b) PCB photo.

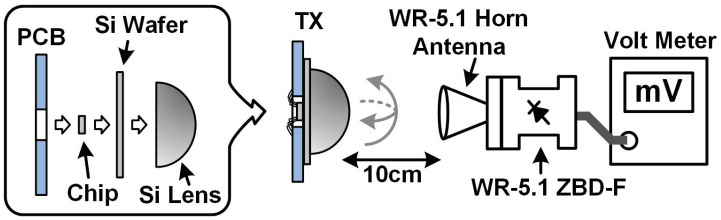
4.4.1 Performance Characterization of the Spatial-Orthogonal ASK Transmitter

The transmitter radiates from the backside of the silicon chip, in order to eliminate the lossy substrate wave, as shown in Fig. 4.18(a), a high-resistivity hemispherical silicon lens with 10 mm diameter is attached. It is worth mentioning that, the chip is located close to the spherical center of the lens, as a result, it has negligible beam collimating effect [5, 37]. For ease of packaging and silicon chip

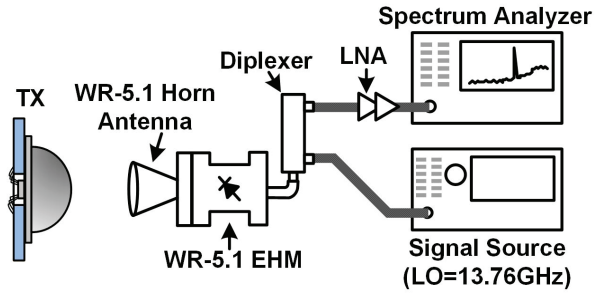
alignment, a high-resistivity silicon wafer (250 μm thick) is placed between the transmitter chip and the silicon lens [3, 4]. The radiation pattern measurement setup is shown in Fig. 4.18(a). The transmitter chip is fixed on a rotary stage, which can rotate in both azimuth and elevation directions. The VDI zero-bias detector, WR-5.1 ZBD-F in Fig. 4.18(a), with a linear polarized conical horn antenna is used to measure the power in each direction. The measured radiation patterns in both spatial channels are shown in Fig. 4.19. Since the same transmitter array is used in both X- and Y-polarized channels with 90° rotation, the radiation pattern is quite similar. The measured directivity is 16.4 dBi and 16.3 dBi, respectively.

In the spectrum measurement, as shown in Fig. 4.18(b), a VDI WR-5.1 even harmonic mixer (EHM) is used to mix the received signal with the 16^{th} harmonic of the 13.76 GHz LO provided by the signal source. The down-converted signal is observed on a spectrum analyzer. The measured down-converted signal spectrum with different data inputs is shown in Fig. 4.20. The CW frequency is measured to be 217.1 GHz and the frequency variation is kept within 0.26 GHz while different input data applied, which proves the effectiveness of the constant-load modulation switch. Fig. 4.20 also shows the channel leakage (Y-polarized channel configured in CW mode with peak output power) is around 30 dB lower, which demonstrates a very good isolation between the two channels.

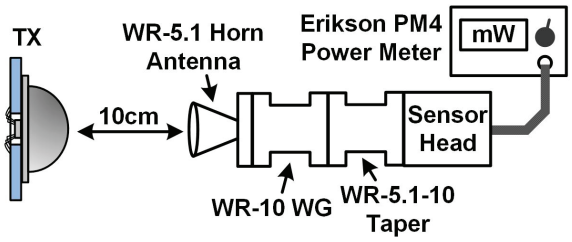
The power measurement setup is shown in Fig. 4.18(c), in which the PM4 calorimeter is used for better precision. For accurate measurement results, the far-field condition needs to be satisfied and standing wave effect must be avoided. Since the horn antenna has a aperture diameter D_{horn} of 8.4 mm [60],



(a)



(b)



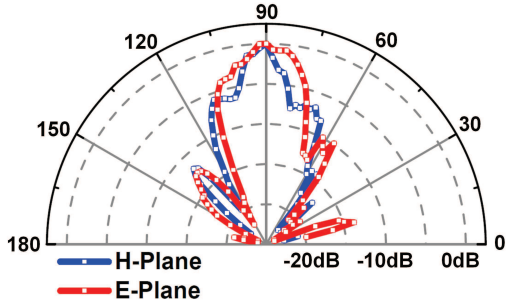
(c)

Figure 4.18: The measurement setups: (a) radiation pattern setup, (b) frequency/spectrum setup and (c) power measurement setup.

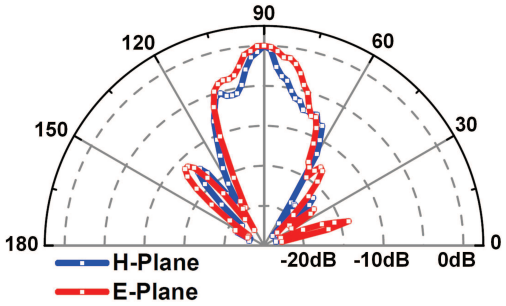
the silicon lens has a diameter D_{Lens} of 5 mm and the silicon wafer thickness T_{wafer} is 250 μm, the far-field distance can be calculated as [37, 61]:

$$D_{far-field} = \frac{2D_{horn}^2}{\lambda_0} - (\sqrt{\varepsilon_{Si}} - 1)(D_{Lens} + T_{wafer}) \approx 8.9cm \tag{4.7}$$

To verify this, in our measurement, the distance between the transmitter and the antenna is first changed from 6 cm to 12 cm, and the received power is measured and shown in Fig. 4.21. The results show that, when the distance is larger than 8 cm, the measurement matches with the Friis equation [62] well, which is close to the theoretical calculation. In the following measurements, a



(a)



(b)

Figure 4.19: The measured radiation pattern of the (a) X-polarized channel and (b) Y-polarized channel.

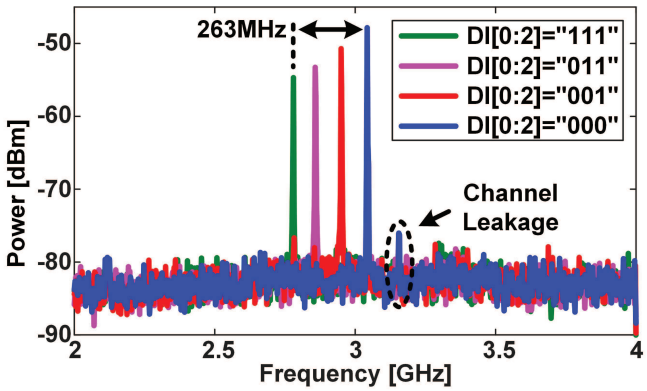


Figure 4.20: The measured spectrum of the down-converted transmitter radiation with different data inputs.

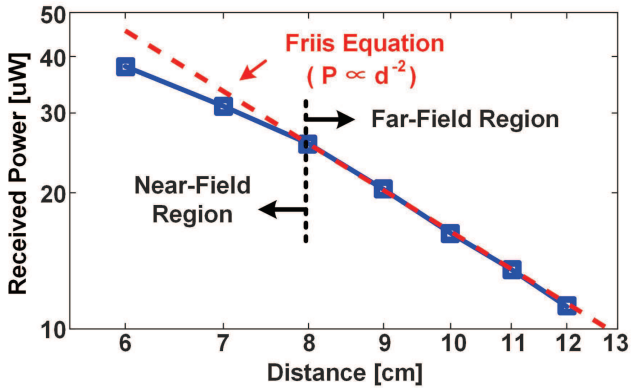


Figure 4.21: The received power measured by the calorimeter at different distances from the transmitter chip. After 8 cm, the results agree with the Friis equation well.

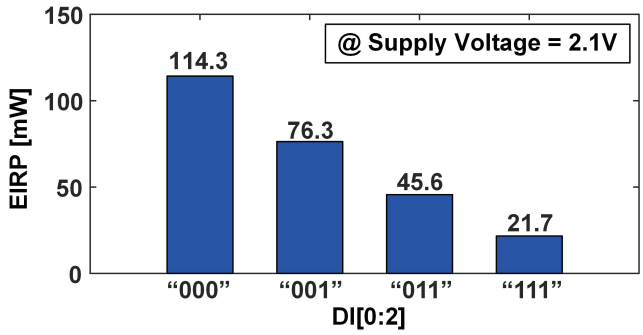
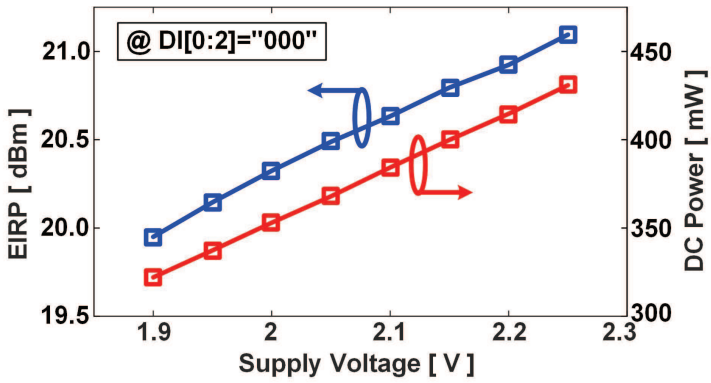
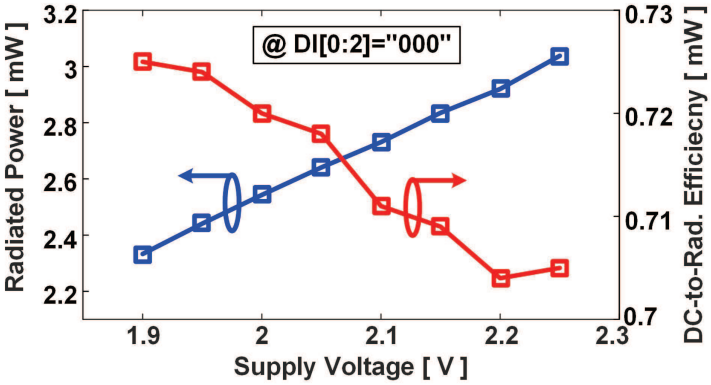


Figure 4.22: The measured X-polarized channel output EIRP with different input codes.

10 cm distance is chosen. With supply voltage fixed at 2.1 V, the transmitter EIRP of the X-polarized channel under each data input is shown in Fig. 4.22. As mentioned previously, the numbers are not equally-spaced due to the antenna directivity of the transmitter slightly changes with data inputs. This distortion can be compensated with adjusting the output power of the transmitter cells in the array. With data input of ”000”, the transmitter is set to CW mode with peak output power. Under this mode, the transmitter EIRP and the associated power consumption of the X-polarized channel under different supply voltages



(a)



(b)

Figure 4.23: The measured X-polarized channel (a) peak EIRP and the associated power consumption, (b) peak radiated power and the associated dc-to-THz-Radiation efficiency at different supply voltages with the input code fixed at "000".

are shown in Fig. 4.23(a). With the results, the total radiated power and dc-to-THz-radiation efficiency can be calculated, as shown in Fig. 4.23(b). The measured peak EIRP and total radiated power in the X-polarized channel are 21.1 dBm and 3.0 mW, respectively. Thanks to the low insertion loss achieved with the proposed modulation switch, a 0.72% peak dc-to-THz-radiation efficiency is achieved. Similarly, performance of the Y-polarized channel is also characterized. The peak EIRP, radiated power and dc-to-THz-radiation efficiency of the Y-polarized channel are 20.9 dBm, 2.9 mW and 0.7%, respectively, which is very

close to the X-polarized channel.

4.4.2 Communication Link Demonstration

To demonstrate the communication link, a conical horn antenna with 21 dBi gain [60] and a fast zero-bias detector (ZBD-F) with NEP of 3 $pW/\sqrt{Hz}$ and responsivity of 3000 V/W [63] are configured as the receiver, as shown in Fig. 4.24. Unfortunately, the ZBD-F is not designed for 50 Ω load and has an output impedance of 1.07 $k\Omega$. The large signal loss caused by this impedance mismatch will significantly increase the noise contribution of the oscilloscope and degrade the overall NEP. With the oscilloscope configured to a 26.5 GHz bandwidth, it has an rms input noise of 0.46 mV [64]. The overall NEP of the receiver can be calculated as [65]:

$$NEP_{RX} = \sqrt{NEP_{det}^2 + (\frac{Z_{o,det} + 50\Omega}{50\Omega} \cdot \frac{v_{n,rms}}{\Re_{det}})^2 \frac{1}{BW}} = 21.3\ pW/\sqrt{Hz} \qquad (4.8)$$

in which, NEP_{det} , $Z_{o,det}$ and $\Re_{det}$ are the NEP, output impedance and responsivity of the ZBD-F; $v_{n,rms}$ and BW are the rms noise and bandwidth of the oscillo-

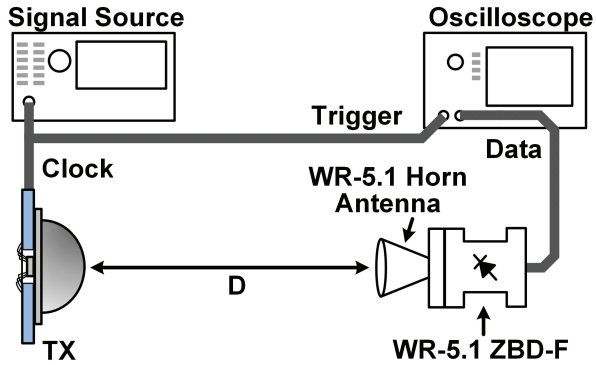
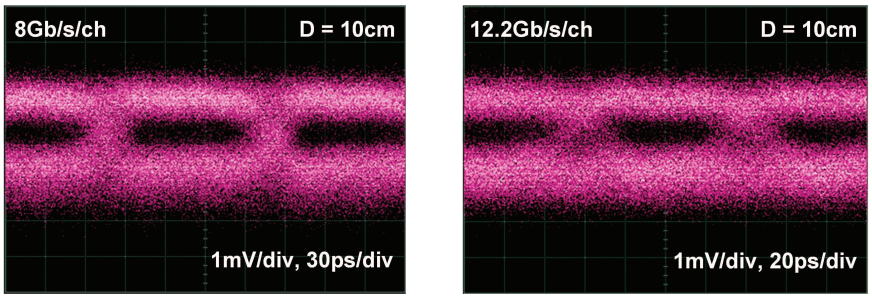
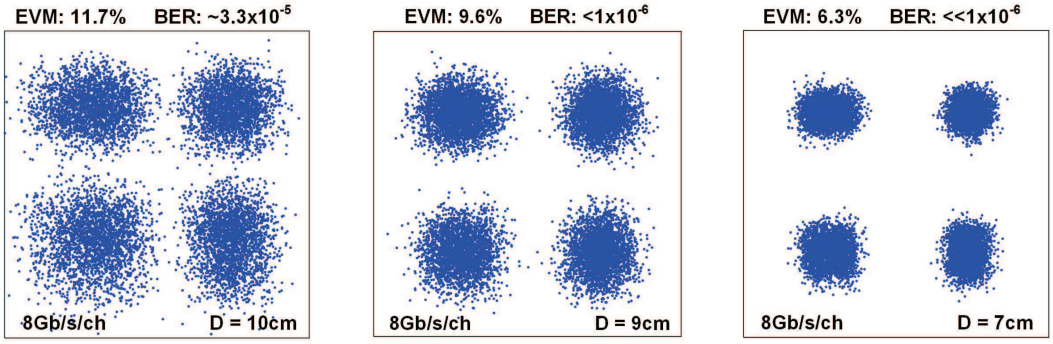


Figure 4.24: The communication link experiment setup. A fast zero-bias detector from VDI is used as the receiver.



(a) (b)

Figure 4.25: The measured X-polarized channel eye diagrams with 10 cm communication range and multi-level function turned off: (a) 8 Gb/s/ch and (b) 12.2 Gb/s/ch. Eye opening is largely affected by the 17 dB SNR drop caused by the impedance mismatch between the ZBD-F and the oscilloscope.



(a) (b) (c)

Figure 4.26: The measured constellation plots at data rate of 8Gb/s/ch with different ranges: (a) 10cm, (b) 9cm and (c) 7cm.

scope. Compared to the original 3 $pW/\sqrt{Hz}$ NEP of the ZBD-F, this impedance mismatch causes a 17 dB SNR drop. This issue can be avoided by inserting a wide-band (> 10 GHz) low-noise buffer with high input impedance and 50 Ω output impedance between the ZBD-F and the oscilloscope, which is difficult to find in commercial components but very possible to custom design. In our experiment, despite this 17 dB SNR drop, with excellent transmitter EIRP achieved, we are still able to demonstrate the communication link without the buffer. First, with a 10 cm communication range and the multi-level function

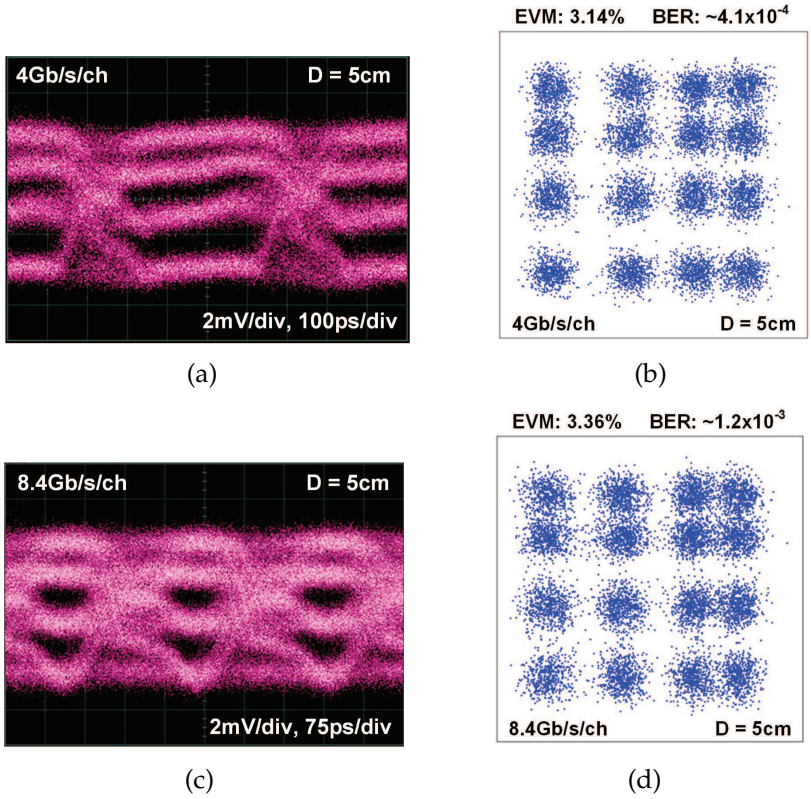
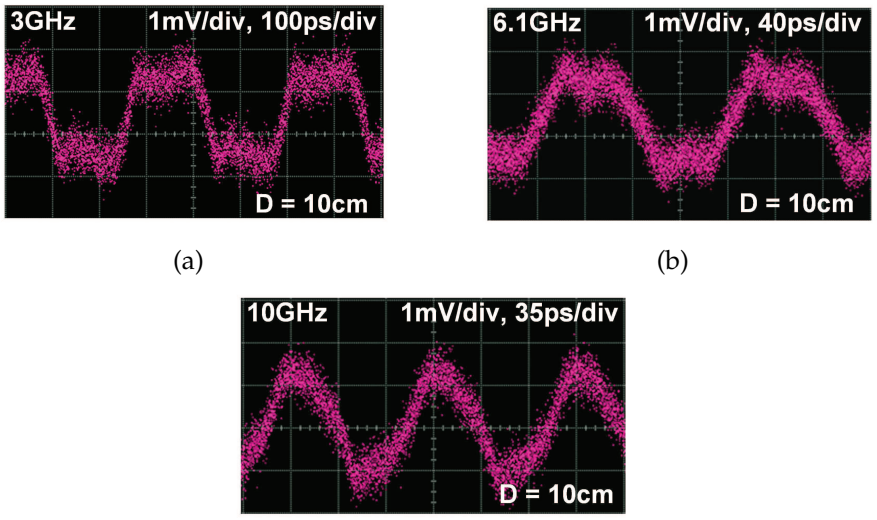


Figure 4.27: The X-polarized channel measurement results with 5 cm communication range and multi-level function turned on: (a) eye diagram and (b) constellation at 4 Gb/s/ch as well as (c) eye diagram and (d) constellation at 8.4 Gb/s/ch. Eye opening and BER are largely affected by the 17 dB SNR drop caused by the impedance mismatch between the ZBD-F and the oscilloscope.

of the transmitter turned off, the measured eye diagrams of the X-polarized channel are shown in Fig. 4.25. The Y-polarized channel eye diagrams are very similar, so they are not shown here. With PRBS input clock set to 4 GHz, a total 16 Gb/s data rate is achieved with a BER of 3.3×10^{-5}. With PRBS clock of 6.1 GHz, 24.4 Gb/s capacity is obtained with BER of 7.2×10^{-5}. Implemented with 0.13-μm CMOS transistors, the PRBS circuit can only work up to a frequency of 6.1 GHz, which limits the highest speed that can be demonstrated. The achieved BER is determined by the power received by the receiver. With

a shorter range, larger power can be received, leading to better SNR and BER as shown in Fig. 4.26. With the limited receiver equivalent NEP, in order to demonstrate the 4-level SO-ASK, the communication range is further reduced to 5 cm for a higher SNR. The measurement results are shown in Fig. 4.27. Beyond 2.1 GHz, the thermometer encoder cannot work properly, consequently, a maximum total data rate of only 16.8 Gb/s is demonstrated. According to Friis equation, by reducing communication range to half, the SNR can increase by 12 dB. However, due to the 5 cm has entered the near-field region according to Fig. 4.21 and the ZBD-F saturates, only ~7 dB increase in SNR is obtained compared to the previous 10 cm range.

In previous experiments, the demonstrated data rate is limited by the PRBS and thermometer encoder circuits, while the transmitter itself has a potential for higher speed. To further estimate the transmitter speed, both PRBS and encoder are by-passed and sinusoidal signals are used directly as data inputs. With single tone frequency changing from 1 GHz to 10 GHz, the receiver output amplitude is observed. Fig. 4.28 gives the results for 3 GHz, 6.1 GHz and 10 GHz, which shows no significant amplitude drop up to 10 GHz. Consequently, the potential modulation speed of the transmitter exceeds 10 GHz. This corresponds to a potential total data rate of at least 40 Gb/s with the multilevel function off and at least 80 Gb/s with the multilevel function on. Due to the 17-dB SNR drop caused by the impedance mismatch between the ZBD-F and the oscilloscope, the demonstrated eye diagram quality, BER and communication range are all significantly affected. Due to the fact that 50 Ω is the standard impedance for commercial high speed components, in our experiment, the impedance mismatch is difficult to avoid. However, in real applications, using custom-designed baseband circuits with high input impedance, this issue



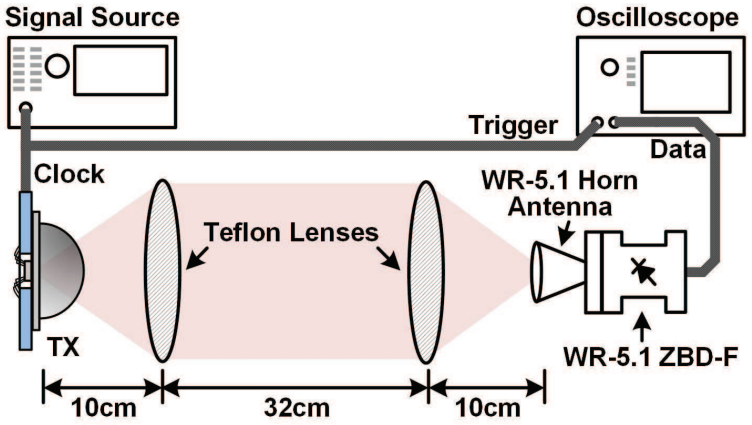
(a) (b)

(c)

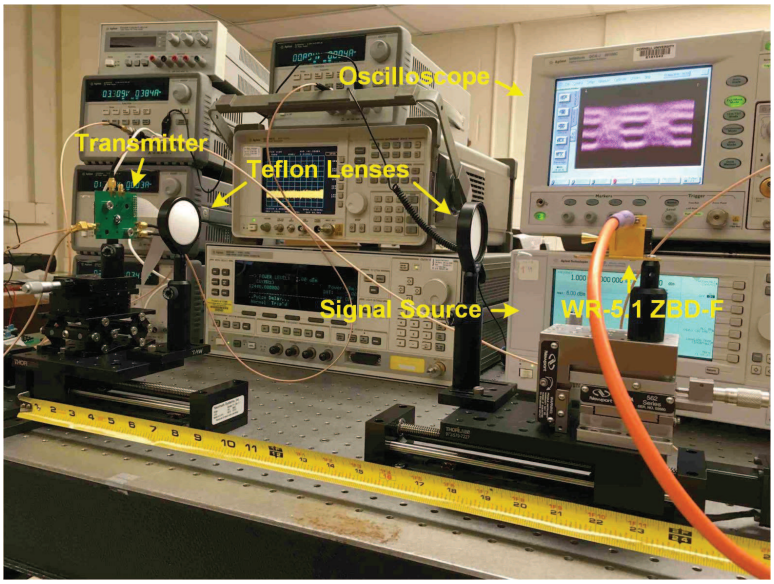
Figure 4.28: Single-tone test of the transmitter with input frequency of: (a) 3 GHz, (b) 6.1 GHz and (c) 10 GHz.

can be eliminated. By de-embedding the 17-dB SNR drop, with the measured transmitter specifications and a targeted BER of 10^{-6}, the proposed transmitter can potentially achieve a calculated communication range of 12.4 cm and 23.1 cm when the multi-level function on and off, respectively. It is also worth mentioning that, beside the impedance mismatch, the receiver in our measurement is not ideal in two other aspects. First, the ZBD-F 1-dB compression point is only -20 dBm [63], but with the high EIRP of the transmitter, more than -10 dBm power can be received at a 5 cm range, which will cause the ZBD-F to saturate and affect the SNR. Second, no baseband filter is implemented, which will cause noise to accumulate within the whole 26.5-GHz oscilloscope bandwidth. If a silicon receiver is to be designed, larger device size can be used for higher 1-dB compression point and baseband filter can be implemented to reduce the noise bandwidth. In fact, state-of-the-art silicon terahertz detectors can achieve an NEP below 10 $pW/\sqrt{Hz}$ [48], which is close to the commercial VDI detectors.

The proposed SO-ASK transmitter consumes a total dc power of 0.45 W inside each spatial channel, in which the oscillators takes 400 mW, the switches and data buffers dissipates 40.5 mW and 9.2 mW, respectively.

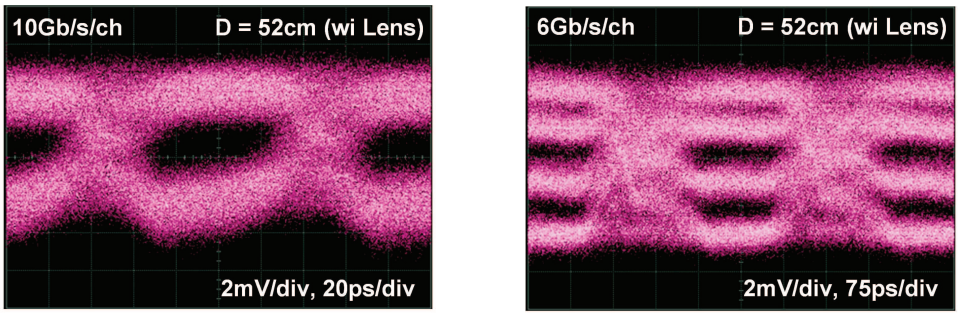


(a)



(b)

Figure 4.29: The Teflon lens system experiment setup: (a) block diagram and (b) photo of the setup. The extended transmitter to receiver distance is 52 cm, which is limited by the length of the linear tracks.



(a) (b)

Figure 4.30: The measured X-polarized channel eye diagrams with the lens system: (a) with PRBS clock of 5 GHz and multi-level turned off, (b) with PRBS clock of 1.5 GHz and multi-level turned on.

4.4.3 Lens System Experiment

To further extend the communication range, Teflon lens system can be used to increase the directivity of the terahertz beam. The setup of the lens system is shown in Fig. 4.29(a), in which two Teflon lenses (10 cm focal length and 5 cm diameter) are used to collimate and focus the transmitted terahertz beam. For ease of alignment, the transmitter and receiver are first placed with a small distance, and then gradually moved apart with two linear tracks, as shown in Fig. 4.29(b). With this system, the communication range can be extended to 52 cm. With PRBS clock of 5 GHz and multi-level turned off, the measured X-polarized channel eye diagram is shown in Fig. 4.30(a). With PRBS clock of 1.5 GHz and multi-level turned on, the eye diagram is shown in Fig. 4.30(b). Theoretically, with good alignment, the range can be further extended, however, in our experiment, the largest distance is limited by the length of the linear tracks.

4.5 Conclusions

A performance summary of the prototype SO-ASK transmitter chip as well as a comparison with other state-of-the-art works are shown in Table 4.3. The proposed oscillator-based self-sustaining transmitter requires no additional inputs other than the input data and dc supply (eg. high frequency LO). The return-path gap based self-feeding oscillators have excellent signal generation efficiency, and the high-speed constant-load switch can modulate the signal with minimum loss, consequently, the transmitter demonstrates excellent power efficiency. With the compact TX cell design, array configuration is easily implemented to enhance the transmitter EIRP. This helps to obtained a 10 cm communication range without using any collimating lens. In [27], a transmitter efficiency is calculated by $Eff = P_{DC}/DataRate$, however, this fails to incorporate the communication range performance of the transmitter, which is very important in real applications. Consequently, another commonly used efficiency metric $Eff = P_{DC}/DataRate/Range$ is calculated in Table 4.3. Please note this efficiency metric does not favor transmitters targeted at longer communication range (D) like this work, since the path loss in wireless communication increases by D^2 instead of D, which means the transmitter power consumption normally needs to increase more than linearly to generate enough output power to compensate the path loss. However, even with demonstrated speed limited by the PRBS and encoder circuits as well as SNR drop caused by the receiver impedance mismatch, this work still shows much higher transmitter efficiency.

With high output power and transmitter efficiency, the proposed system can be used for chip-to-chip communication and short-range ultra-fast device-to-device data exchange. With external collimating lens system to extend the com-

munication range, it also has the potential to be use for future high-speed indoor point-to-point communication.

Table 4.3: Performance Summary and Comparison

Reference	JSSC 2014 [53]	JSSC 2015 [27]	ISSCC 2016 [54]	TMTT 2016 [73]	TMTT 2016 [74]	This Work	
Frequency (GHz)	210	240	275-305	165	300	217	
Source Type	Oscillator	Frequency Multiplier	Off-Chip	Oscillator	Frequency Multiplier	Oscillator	
Output Power (dBm)	4.6	0	-14.5	-1.7	-4.4	4.8 (X-pol) 4.6 (Y-pol)	
EIRP (dBm)	5.13	1	\	\	21.86	21.1 (X-pol) 20.9 (Y-pol)	
Modulation Scheme	OOK	QPSK/BPSK	32-QAM	OOK	QPSK/QAM	SO-ASK	4-Level SO-ASK
Data Rate (Gb/s)	10 (3)	16	17.5×6 (4)	9.4	2.73	24.4 (demo) (1) > 40 (estimated)	16.8 (demo) (1) > 80 (estimated)
Demonstrated Range (cm)	\ (3)	1 (Wireless)	0 (Probed)	2.3 (Waveguide)	15 (Wireless)	10 (2) (Wireless)	5 (2) (Wireless)
DC Power (mW)	240	220	1400	6.4	1030	450×2	
Area (mm^2)	3.5 (Chip)	2 (Chip)	6 (Chip)	0.46 (Chip)	1.7 (Chip)	0.096 (TX Cell) 2.8 (Chip)	
Technology [f_T / f_{max} (GHz)]	32nm SOI [250 / 320]	65nm CMOS [NA / NA]	40nm CMOS [NA / 280]	65nm CMOS [200 / 240]	130 nm SiGe [300 / 450]	130 nm SiGe [220 / 280]	
Efficiency (pJ/bit/cm) (5)	\	13.8	\	\	25.2	3.7 (1,2)	
Silicon Lens Used	\	\	\	\	Collimating (both RX and TX)	Non-collimating	

(1) Demonstrated data rate is limited by the speed of the on-chip PRBS and thermometer encoder circuits.
(2) Demonstrated range is degraded by the 17 dB SNR drop caused by the impedance mismatch between the ZBD-F and oscilloscope.
(3) Not demonstrated, calculated from receiver bandwidth. (4) Six frequency channels combined. (5) *Efficiency* = P_{DC}/*Data Rate/Range*.

CHAPTER 5

AN ENTIRELY-ON-CHIP FREQUENCY STABILIZATION FEEDBACK MECHANISM FOR TERAHERTZ SOURCES

In coherent terahertz (THz) systems, such as the imager system described in Chapter 3, signal sources with stable frequencies are needed. At low frequencies, phase-locked loops (PLLs) are often designed for this purpose. However, adopting PLLs structures into THz band is facing many obstacles. In this chapter, a novel frequency-stabilization mechanism suitable for THz sources is introduced, which can eliminate the need for off-chip references as well as frequency dividers, achieving much lower system integration cost and power consumption.

5.1 Introduction

The THz band has shown its unique potentials in a variety of applications, such as high-resolution non-ionizing imaging [4], ultra-high-speed communication [7], as well as high-sensitivity spectroscopy [17]. These applications have great value in many different areas, such as scientific research, military use as well as industrial production. Integrating THz systems with a commercial CMOS or BiCMOS technology is quite attracting for the potential in significant reduction of size and cost. Consequently, silicon terahertz electronics has drawn lots of research efforts recently.

All of the aforementioned applications need signal sources to generate the THz waves. Frequency stability is also often required to allow coherent operations [4, 27, 28]. Currently, there are two major methods to generate THz

signal: frequency multipliers and harmonic oscillators [29]. With high-quality and wideband drive signal, frequency multipliers can provide frequency-locked output with large tuning range. However, to push the frequency into THz range, multi-stage architecture and inter-stage power amplification are often needed [27], which results in low power efficiency and large area. To achieve better efficiency and size for THz system integration, harmonic oscillators can be used [1]. However, due to supply noise and ambient environment change, free running THz oscillators exhibit large spectral linewidth and frequency drift. As a result, frequency stabilization is required. Previous works have demonstrated THz PLLs for this purpose. In [45], a 300-GHz PLL with 7.8% tuning range is demonstrated. A triple-push oscillator is used to send out its third harmonic as output and a injection-locking frequency divider (ILFD) with three-phase injection is adopted. It burns 376 mW dc power, generating only -14 dBm probed THz power. To produce more power for real applications, a new architecture is proposed in [2]. A 4×4 radiator array dedicated for high-efficiency THz radiation generation is designed, and a 160 GHz PLL is used to inject-lock the radiator array for frequency locking. This work is able to generate a 5.2-dBm radiated power at 320 GHz with a 0.54% dc-to-THz efficiency. However, due to the large fundamental swing in the radiator cells and limited injection power from the PLL, only 0.2 GHz locking range is achieved. In [71], a 560-GHz PLL is introduced, in which prime and auxiliary triple-push oscillators as well as two stages of injection-locking dividers are included. Sub-sampling phase-detection scheme is used to enhance the output phase noise. With 172 mW dc power, a -27-dBm radiated power is measured.

Unfortunately, PLL design encounters big challenges when frequency goes into THz range:

(i) At low offset frequency, phase noise of the reference is multiplied by N^2 to the output [67], where N is the total division ratio. Since N is very large in THz PLLs, normally in the order of $10^3 \sim 10^4$ [2, 45, 71], a high-quality off-chip crystal oscillator is needed to keep the noise contribution low enough. Use of the crystal oscillator increases the total system cost by a lot.

(ii) Injection-locking frequency dividers (ILFDs) in THz range provide insufficient locking range, which limits the achievable output frequency range. In order to obtain a wider ILFD locking range, higher injection power or multi-phase injection [45, 72] is needed, which significantly increases the total power consumption.

(iii) The large division ratio, N, also causes significant VCO noise folding, potentially degrades the output in-band phase noise [68].

In this chapter, an entirely-on-chip frequency-stabilization feedback mechanism suitable for THz sources is presented, which utilizes the frequency response of the on-chip passive EM structures to implement frequency detection. This scheme eliminates the need for both frequency dividers and off-chip crystal oscillators, resulting in much lower system cost and power consumption. To verify this idea, a 301.7-to-331.8-GHz source prototype is designed in the STMicroelectronics 0.13-μm SiGe:C BiCMOS technology. The source achieves a power consumption of only 51.7 mW. The measured phase noise is -71.1 and -75.2 dBc/Hz at 100 kHz and 1 MHz offset, respectively. A -13.9-dBm probed output power is also achieved.

5.2 Principle and Analysis of the Proposed Fully On-chip Frequency Stabilization Mechanism

In order to stabilize the output frequency of a THz oscillator, a mechanism is needed for sensing its instant output frequency and generate an feedback control signal. In this section, the proposed mechanism will be discussed in detail.

5.2.1 Frequency Sensing Based on Passive EM Structures

Almost all passive EM structures exhibit frequency-dependent responses, in principle, all these responses can be utilized to sense the frequency. However, in order to get a high output signal-to-noise ratio, or good phase noise, a high-gain sensing mechanism is needed.

The proposed frequency detection mechanism is shown in Fig. 5.1. The input signal, P_{in}, is split into two paths. The upper path is mainly composed of a bandpass filter, whose phase-frequency response exhibits a steep slope within the passband. Consequently, phase shift of the upper path is highly dependent on the input frequency. On the contrary, phase shift of the lower path does not change much with frequency. As a result, the phase difference of P_3 and P_4 is a strong function of frequency. This means after power combining, the output power P_{det} can be used as a frequency detection product. A power detector then converts P_{det} to I_{det}, which later is used to generate the VCO control feedback.

The core of this frequency detection mechanism is the bandpass filter. Shown in Fig. 5.2(a) is a third-order bandpass filtered implemented using capacitively-

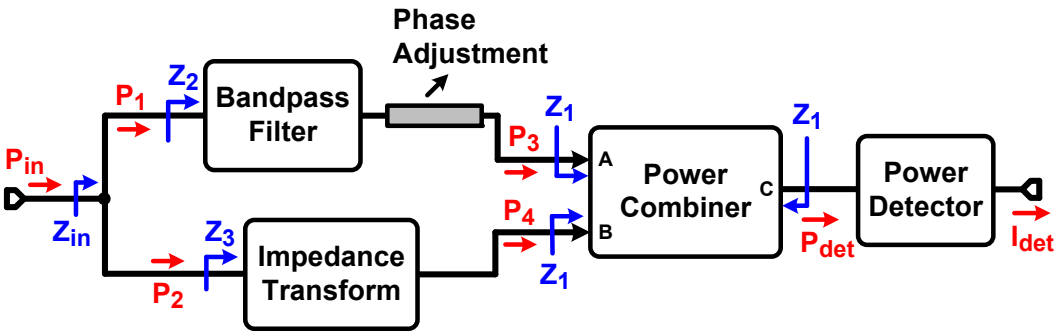
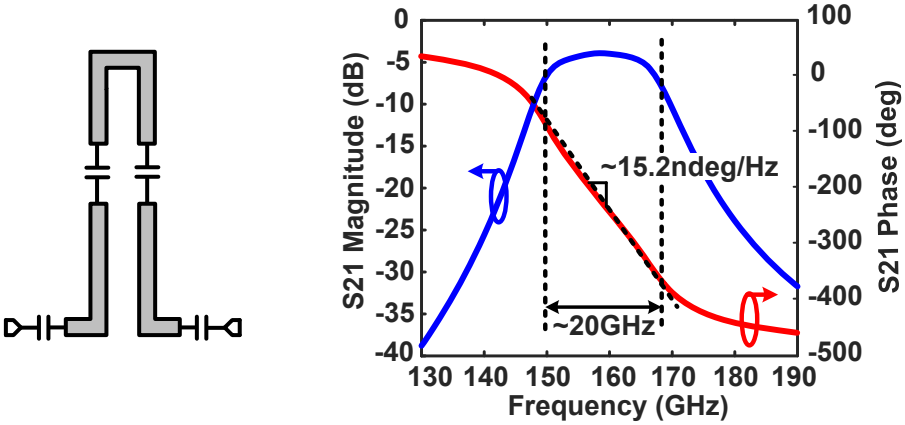


Figure 5.1: The proposed frequency detection scheme.



(a) (b)

Figure 5.2: Bandpass filter using capacitive coupled series resonators: (a) structure and (b) simulated frequency response.

coupled series resonators [69]. It has three transmission line sections (approximately $\lambda/2$ long) and four capacitive gaps between them [modeled as lump capacitors in Fig. 5.2(a)]. This type of filters are convenient to implement on chip and suitable for THz design, since they are basically sections of transmission lines. With proper design, the simulated bandpass filter frequency response is shown in Fig. 5.2(b). Within the passband of around 20 GHz, phase delay of the filter varies significantly with frequency, which is helpful to achieve a high-gain frequency detection.

A typical Wilkinson power combiner can be described using the s-parameters shown below:

$$[\mathbf{S}]_{combiner} = \sqrt{\frac{\gamma}{2}} \begin{bmatrix} 0 & 0 & -j \\ 0 & 0 & -j \\ -j & -j & 0 \end{bmatrix}, \tag{5.1}$$

in which, γ is the power loss of the combiner. Under perfect matching at all the ports, the output power P_{det} is written as:

$$\begin{aligned} P_{det} &= \frac{\gamma}{2}|(\sqrt{P_3}e^{-j\Delta\phi} + \sqrt{P_4})|^2 \\ &= \frac{\gamma}{2}(\alpha P_1 + \beta P_2 + 2\sqrt{\alpha\beta P_1 P_2}\cos\Delta\phi), \end{aligned} \tag{5.2}$$

in which, $\Delta\phi$ is the phase difference of the signals at the input ports of the power combiner; α and β are the power loss of the upper and lower paths, respectively. Due to the higher insertion loss of the bandpass filter, α is smaller than β. The frequency detection gain $|K_{det}|$ can be expressed as:

$$|K_{det}| = |\frac{dP_{det}}{df}| = |\frac{dP_{det}}{d\Delta\phi}| \cdot |\frac{d\Delta\phi}{df}|. \tag{5.3}$$

Since $|d\Delta\phi/df|$ is mainly determined by the bandpass filter, now it is desired to maximize $|dP_{det}/d\Delta\phi|$. Using (5.2), it is not difficult to derive:

$$\begin{aligned} |\frac{dP_{det}}{d\Delta\phi}| &= |-\gamma\sqrt{\alpha\beta P_1 P_2}\sin\Delta\phi| \\ &\leqslant \gamma\sqrt{\alpha\beta}\sqrt{(\frac{P_1+P_2}{2})^2} = \frac{\gamma}{2}\sqrt{\alpha\beta}P_{in}. \end{aligned} \tag{5.4}$$

It shows $|dP_{det}/d\Delta\phi|$ takes the maximum value when $P_1 = P_2$, meaning that the maximum frequency detection gain happens when the power is divided evenly between the upper and lower paths. However, as will be discussed in Section 5.3, there exists a tradeoff among responsivity, output noise and compression point in the power detector design, and it is also desired to have a lower maximum P_{det}. Fig. 5.3 shows the simulated $dP_{det}/d\Delta\phi$ and maximum P_{det} with

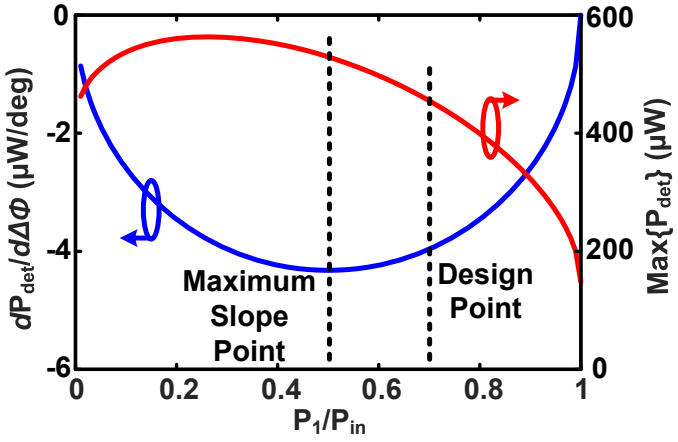


Figure 5.3: The simulated $dP_{det}/d\Delta\phi$ and maximum P_{det} under different power division ratios between the upper and lower paths. In this simulation, $\alpha = 0.32$, $\beta = 0.89$, $\gamma = 0.93$, $P_{in} = 1$ mW.

different power division ratios between the two paths. In this design, around 70% of the input power is sent to the upper path, so that after experiencing different loss in the two paths, P_3 is roughly equal to P_4. In this way, beside obtaining a near-maximum $|d\Delta\phi/df|$, a reasonable maximum P_{det} is obtained to facilitate the power detector design. To realize this power division ratio, in the lower path, a impedance transform block is inserted to change the lower path input impedance from $Z_1 = 45\ \Omega$ to $Z_3 = 115\ \Omega$. It is worth mentioning that, phase-frequency response of this impedance transformation slightly reduces the detection gain and increases the monotonic frequency range of P_{det}. To ensure P_{det} is a monotonic function of frequency and optimum detection gain happens inside the VCO bandwidth, as shown in Fig. 5.1, an additional transmission line section is added to adjust the phase shift of the upper path.

In this scheme, the VCO frequency is referenced to the phase-frequency response of the bandpass filter, which is not sensitive to supply voltage noise and much less sensitive to ambient environment change. Since all these EM structures are made of top metal with large geometries, they are also much less sen-

sitive to process variation.

5.2.2 System Modeling

Using the proposed frequency-detection scheme, block diagram of the frequency-stabilization feedback loop is shown in Fig. 5.4. A model of this system is drawn in Fig. 5.5. The loop gain of the system is derived as:

$$G_{loop}(s) = -K_{det}\Re_{pd}K_{VCO}Z_{LF}(s) \tag{5.5}$$

in which, K_{det} is the frequency detection gain, $\Re_{pd}$ is the responsivity of the power detector and $Z_{LF}(s)$ is the transfer function of the loop filter. Since the feedback senses frequency instead of phase, the pole at origin introduced by the VCO is outside the loop. However, in order to suppress the VCO phase noise at low offset frequencies, at least one pole at origin is necessary. To provide such a pole at origin, as shown in Fig. 5.4, in the loop filter, a large capacitor C_1 is placed in parallel. Capacitor C_2 and resistors R_1 and R_2 create an additional pole and zero. With this loop filter implementation, in steady state, we have $I_{tot} = I_{tune} - I_{det} = 0$. As a result, with different I_{tune} inputs, the steady-state I_{det} is

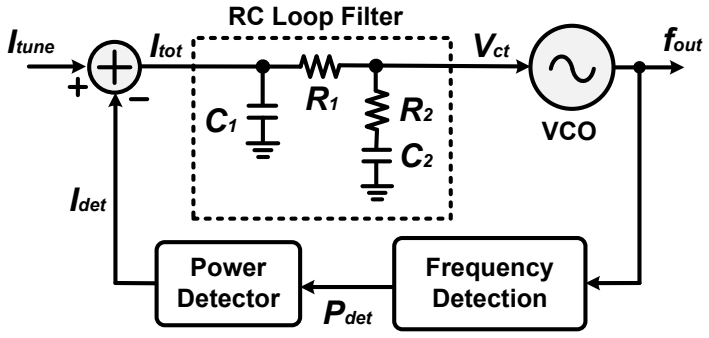


Figure 5.4: Block diagram of the proposed frequency-stabilization feedback loop.

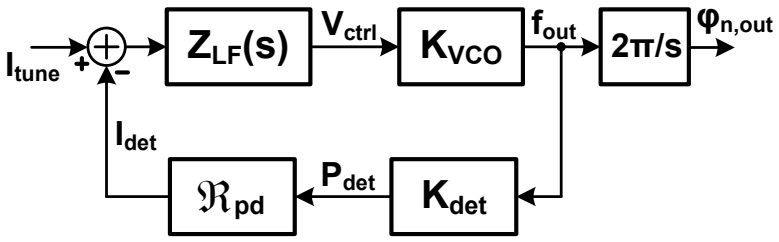


Figure 5.5: Model of the the frequency-stabilization feedback loop.

set, so is the output frequency.

Approximately, transfer function of the loop filter can be derived as ($C_1 \gg C_2$):

$$\begin{aligned} Z_{LF}(s) &\approx \frac{1}{sC_1} \cdot \frac{1 + sC_2R_2}{1 + sC_2(R_1 + R_2)} \\ &= \frac{1}{C_1} \cdot \frac{R_2}{R_1 + R_2} \cdot \frac{s + 1/\tau_z}{s(s + 1/\tau_p)} , \end{aligned} \tag{5.6}$$

in which, $\tau_z = C_2R_2$ and $\tau_p = C_2(R_1 + R_2)$. With (5.5) and (5.6), the loop gain is given by:

$$G_{loop}(s) = -K_0 \frac{s + 1/\tau_z}{s(s + 1/\tau_p)} , \tag{5.7}$$

$$K_0 = \frac{K_{det}\Re_{pd}K_{VCO}}{C_1} \cdot \frac{R_2}{R_1 + R_2} . \tag{5.8}$$

Now the close-loop transfer function can be derived as:

$$\begin{aligned} H_{cl}(s) &= \frac{f_{out}}{I_{tune}}(s) = \frac{K_{VCO}Z_{LF}(s)}{1 - G_{loop}(s)} \\ &= \frac{K_0}{K_{det}\Re_{pd}} \cdot \frac{s + 1/\tau_z}{s^2 + (K_0 + 1/\tau_p)s + K_0/\tau_z} . \end{aligned} \tag{5.9}$$

With careful design, the root locus of the feedback system is shown in Fig. 5.6. At the designed K_0, the close-loop system has two poles with damping factor ξ close to 0.707 for fast settling. Since the whole root locus is in the $\xi < 0.707$ region (left side of the green dash line in Fig. 5.6), the system is always stable

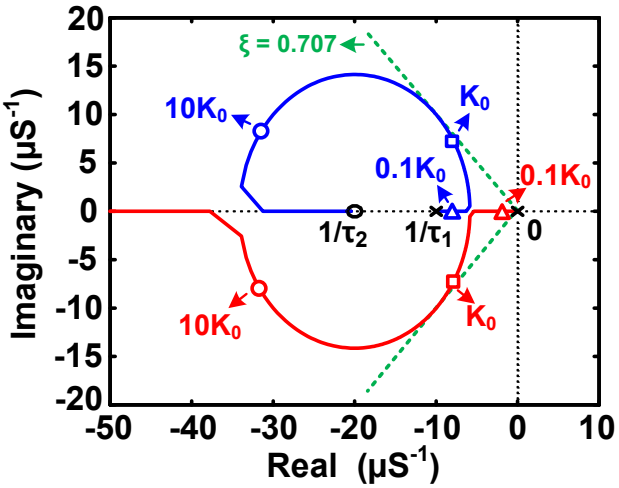


Figure 5.6: The simulated root locus of the frequency stabilization feedback loop. The loop is always stable even if K_0 deviates significantly from the designed value.

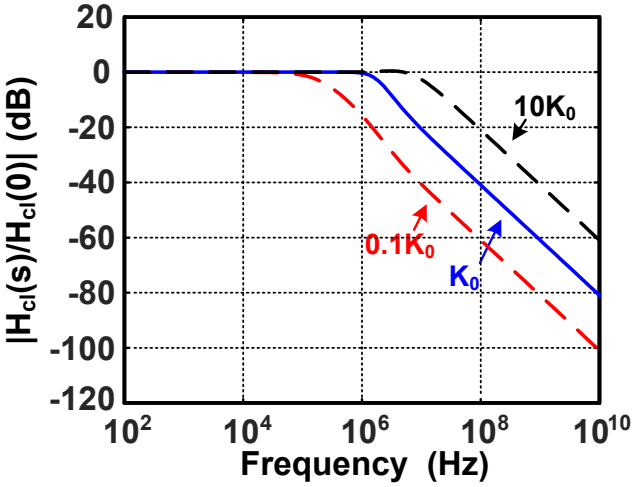


Figure 5.7: The simulated close-loop frequency response of the frequency stabilization feedback loop. K_0 variation changes the close-loop bandwidth.

with enough phase margin regardless of K_0. This is very helpful, since the implemented K_{VCO} as well as the power detector responsivity, $\Re_{det}$, may vary a lot compared to simulation. However, it is worth mentioning that, changing of K_0 will affect the close-loop bandwidth of the system, as shown in Fig. 5.7.

5.2.3 Noise Analysis

The model used to analyze the output noise of the frequency-stabilization feedback system is shown in Fig. 5.8. In this system, noise sources include the VCO phase noise, thermal noise of the passive frequency-detection EM structures, noise of the power detector as well as thermal noise of R_1 and R_2 in the RC loop filter. Also, in reality, the input tuning current, I_{tune}, also introduces noise (denoted as $i_{n,tune}$ in Fig. 5.8). To reduce noise contribution of this part, a low-noise off-chip current source is used.

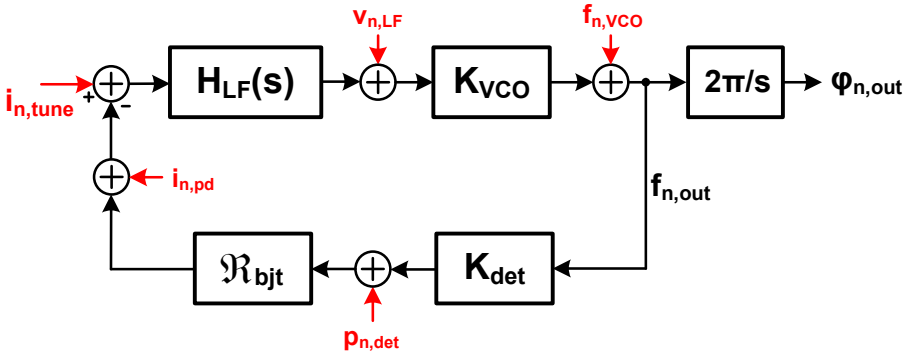


Figure 5.8: Noise model of the frequency-stabilization feedback loop.

Since noise of the passive EM structures is much lower than the active devices used in other blocks, noise contribution of this part can be neglected. As a result, the total output phase noise can be approximately written as:

$$\begin{aligned} S_{\phi_{n,out}}(f) \approx\ & S_{\phi_{n,VCO}}(f)\left|\frac{\phi_{n,out}}{\phi_{n,VCO}}(j2\pi f)\right|^2 \\ & + S_{v_{n,LF}}(f)\left|\frac{\phi_{n,out}}{v_{n,LF}}(j2\pi f)\right|^2 \\ & + S_{i_{n,tune}}(f)\left|\frac{\phi_{n,out}}{i_{n,tune}}(j2\pi f)\right|^2 \\ & + S_{i_{n,pd}}(f)\left|\frac{\phi_{n,out}}{i_{n,pd}}(j2\pi f)\right|^2 . \end{aligned} \tag{5.10}$$

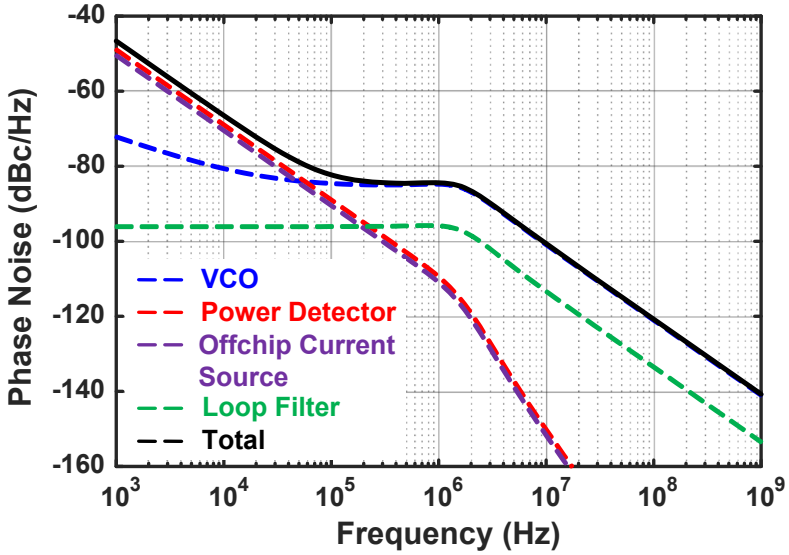


Figure 5.9: The simulated phase noise and contribution from each noise source.

It is not difficult to derive the followings:

$$\frac{\phi_{n,out}}{\phi_{n,VCO}}(j2\pi f) = \frac{f_{n,out}}{f_{n,VCO}}(j2\pi f) = \frac{1}{1 - G_{loop}(j2\pi f)} \tag{5.11}$$

$$\frac{\phi_{n,out}}{v_{n,LF}}(j2\pi f) = \frac{K_{VCO}}{1 - G_{loop}(j2\pi f)} \cdot \frac{1}{jf} \tag{5.12}$$

$$\frac{\phi_{n,out}}{i_{n,tune}}(j2\pi f) = \frac{\phi_{n,out}}{i_{n,pd}}(j2\pi f) = \frac{-G_{loop}(j2\pi f)}{1 - G_{loop}(j2\pi f)} \cdot \frac{1}{jfK_{det}\Re_{pd}} . \tag{5.13}$$

Expression of $G_{loop}(j2\pi f)$ can be found in (5.7). It can be seen from (5.13) that, noise contribution of both the power detector and the input tuning current decreases with K_{det} and $\Re_{pd}$, which justifies our previous effort in achieving a large frequency-detection gain. The output voltage noise spectrum of the loop filter can be calculated as:

$$\begin{aligned} S_{v_{n,LF}}(f) = {} & 4KTR_1 \left| \frac{(1 + j2\pi f C_2 R_2)C_1}{(C_1 + C_2) + j2\pi f C_1 C_2 (R_1 + R_2)} \right|^2 \\ & + 4KTR_2 \left| \frac{(1 + j2\pi f C_1 R_1)C_2}{(C_1 + C_2) + j2\pi f C_1 C_2 (R_1 + R_2)} \right|^2 \end{aligned} \tag{5.14}$$

With (5.10)–(5.14), simulated noise spectrum $S_{\phi_{n,out}}$ and $S_{i_{n,pd}}$, as well as the off-chip tuning current noise spectrum $S_{i_{n,tune}}$ from data sheet, the noise contribution

from each part as well as the total output phase noise of the system is plotted in Fig. 5.9. Due to the system senses frequency instead of phase, the VCO frequency-to-phase integration ("$2\pi/s$" in Fig. 5.8) is outside the loop, and the in-band phase noise of the output also shows a -20dB/dec slope. Similar to conventional PLLs, the out-of-band noise is dominant by the VCO phase noise and the in-band phase noise is dominant by noise contributions of the frequency or phase sensing blocks (PFD, charge pump and frequency reference in conventional PLLs and power detector, input tuning current in this design).

5.3 Design of the Circuit Prototype

Architecture of the prototype source is shown in Fig. 5.10. The VCO has a fundamental frequency centered at 79 GHz. Its second harmonic is sent to the front-end (FE) and back-end (BE) buffer amplifiers. The FE buffer drives a frequency doubler, which generates the 316 GHz output. The BE buffer sends the signal for frequency detection and generation of the VCO control feedback, V_{ctrl}. An off-chip low-noise current source provides the input tuning current, I_{tune}, to set the output frequency. Next, design of detailed circuit blocks will be discussed.

5.3.1 Passive Frequency Detection EM Structures

As shown in Fig. 5.10, majority of the passive EM structures are implemented with transmission lines. To achieve good quality factor and compact size, G-CPW transmission lines are adopted. The signal line is implemented with the 3-μm thick top copper (M6), while an overlapped M1-to-M3 ground plane is

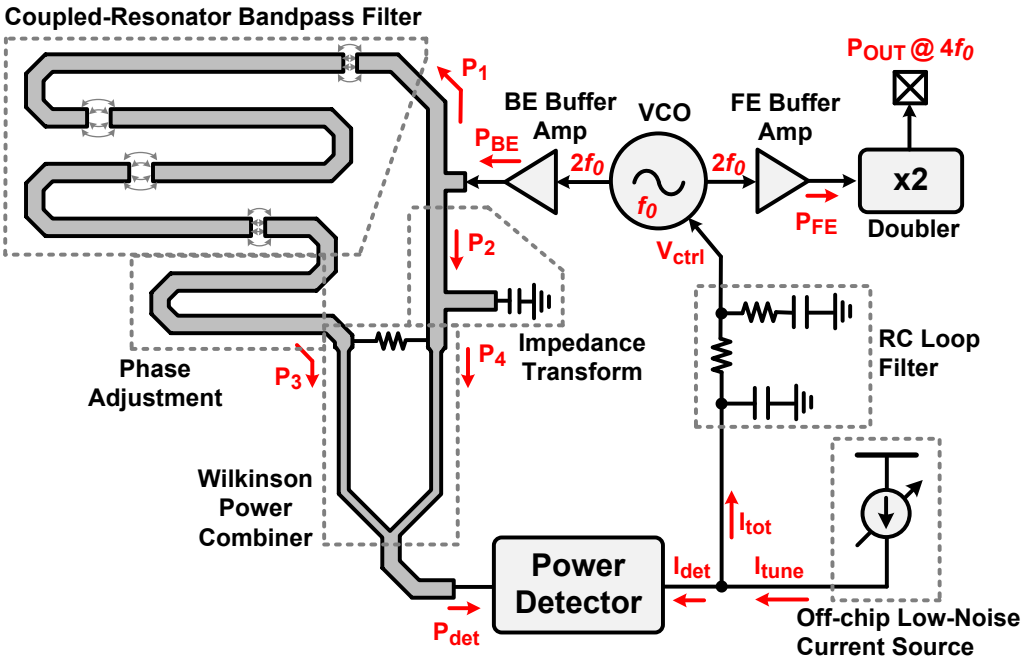


Figure 5.10: Architecture of the 316 GHz prototype source.

placed underneath and M1-to-M6 stacked ground walls are placed on the two sides. By changing width of the signal line, the characteristic impedance can be implemented is from 35 Ω to 68 Ω.

Implementation of the coupled-resonator bandpass filter is shown in Fig. 5.11, which is formed with three series sections of transmission lines (Z_0 = 45Ω) near $\lambda/2$ and four coupling capacitor. To obtain a passband of 20 GHz near the center frequency of 159 GHz, electrical length of the transmission line sections

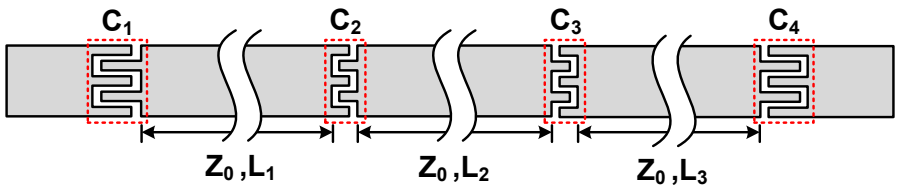


Figure 5.11: Bandpass filtered implemented using capacitive-gap coupled series resonators.

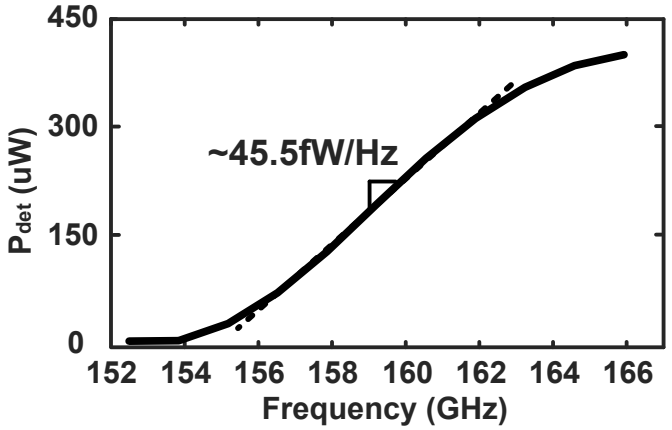


Figure 5.12: The simulated frequency detection gain, assuming an input power of 1 mW.

as well as value of the capacitors can be found as [69]:

$$L_1 = L_3 = 0.414\lambda\ , \quad L_2 = 0.444\lambda \tag{5.15}$$

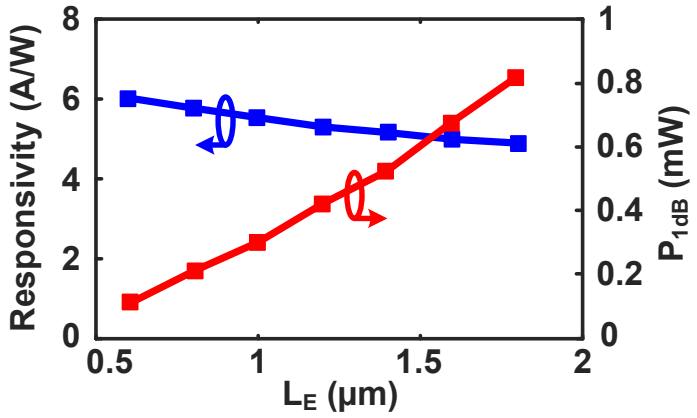
$$C_1 = C_4 = 9.96fF\ , \quad C_2 = C_3 = 4.07fF\ . \tag{5.16}$$

The coupling capacitors are implemented with the cross-finger metal-oxide-metal (MOM) structure. Top copper (M6) is used to enhance their quality factor as well as to minimize parasitic capacitances to the ground.

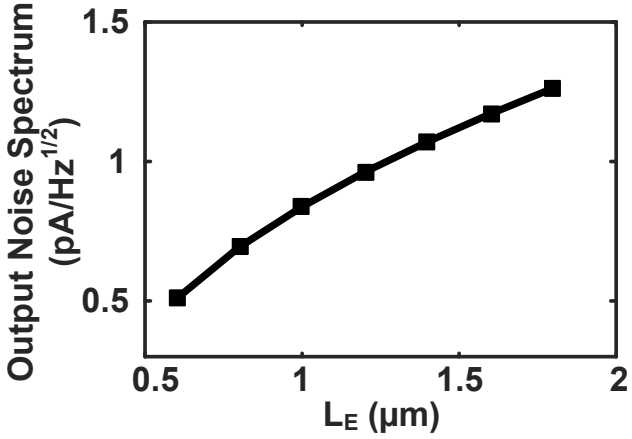
The power combiner used in this design is a classic Wilkinson combiner as shown in Fig. 5.10. The simulated frequency detection gain, K_{det}, using these passive EM structures is about 45.5 fW/Hz, as shown in Fig. 5.12. It is noteworthy that, there is a tradeoff between the frequency detection gain and the operating bandwidth. As shown in (5.2), P_{det} is a periodic function with $\Delta\phi$. For the system to work properly, $\Delta\phi$ needs to be limited between $2k\pi$ and $(2k+1)\pi$, where k is an integer. In principle, for the bandpass filter design, we can increase the filter order or decrease the passband to increase $|d\Delta\phi/df|$ and achieve a higher total frequency detection gain, however, the frequency detection range will be sacrificed.

5.3.2 Power Detector

In this design, an npn bipolar transistor is used as the power detection device for its lower noise contribution and good nonlinear characteristics. When choosing size of the transistor, tradeoff exists among the achievable responsivity, power handling and noise performances. To elaborate this point, simulations are per-



(a)



(b)

Figure 5.13: The simulated performance of the power detector using different size of BJT transistors: (a) Responsivity and 1-dB compression point as well as (b) output current noise spectral density.

formed on different sizes of bipolar transistors. In this process, the transistor emitter width is fixed to be $W_E = 0.27\ \mu m$, but we can choose different emitter length, L_E, and number of emitters, n_{be}. Fixing $n_{be} = 2$ and biasing point, Fig. 5.13 shows the simulated responsivity, 1-dB compression point and the output current noise spectrum density for different L_E. From the results, we can see that, in order to handle higher input power, a larger device is needed, however, at the cost of slightly lower responsivity and much higher output noise. Intuitively, a larger device has a lower input impedance, which means for the same amount of input power, lower voltage swing is resulted. As a result, the device enters saturation slower. However, at the same biasing point, a larger device generates higher shot noise. The responsivity also slightly drops due to less nonlinear behavior. Due to this tradeoff, as mentioned previously in Section 5.2, while designing the frequency-detection EM structures, beside the frequency detection gain, we also need to care about the maximum input power that needs to be handled by the power detector.

Shown in Fig. 5.14 is the schematic of the power detector, in which $L_E = 1.4\ \mu m$ is chosen. A shunt-stub matching network is used to transform the ca-

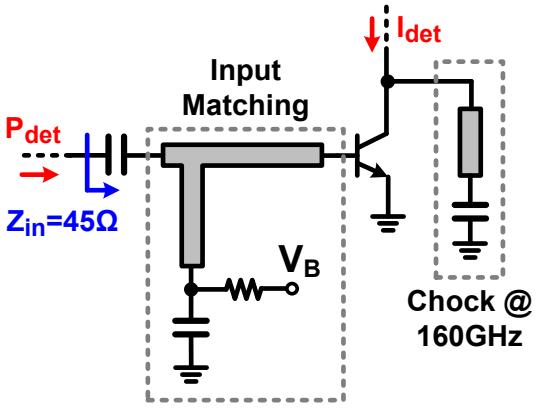


Figure 5.14: Schematic of the power detector.

pacitive base impedance into the desired 45Ω. The 160-GHz chock at the collector reflects the 160-GHz signal back to the device to enhance the responsivity. According to simulation, the achieved responsivity, 1-dB compression point and output noise current density of the power detector is 5 A/W, 540 μW and 1.07 $pA/\sqrt{Hz}$, respectively.

5.3.3 VCO and Buffer Amplifiers

To obtain a wider frequency tuning range, a differential Colpitts oscillator is used in this design [5]. As shown in Fig. 5.15, cascode transistors Q_3 and Q_4 are placed on top of the core transistors Q_1 and Q_2 to provide the required low impedance at collector of Q_1 and Q_2. Tail current sources M_1 and M_2 provide the bias current. Transmission lines TL_1 and TL_2 transform the capacitive impedance at the drain of M_1 and M_2 into a high impedance to avoid the loading effect to the VCO core. The extracted second harmonic is sent to both the front-end and back-end buffer amplifiers. A cascode topology is used in the buffer amplifiers design for better reverse isolation and stability. Beside the varactor, the VCO frequency can be additionally tuned by changing the bias of M_1 and M_2 (V_G in Fig. 5.15). According to the simulation, the total output tuning range of the VCO is 18 GHz around a center frequency of 158 GHz. The K_{VCO} is simulated to be 5.2 GHz/V. The generated power at the front-end and back-end buffer output is 1.5 mW and 1.3 mW, respectively.

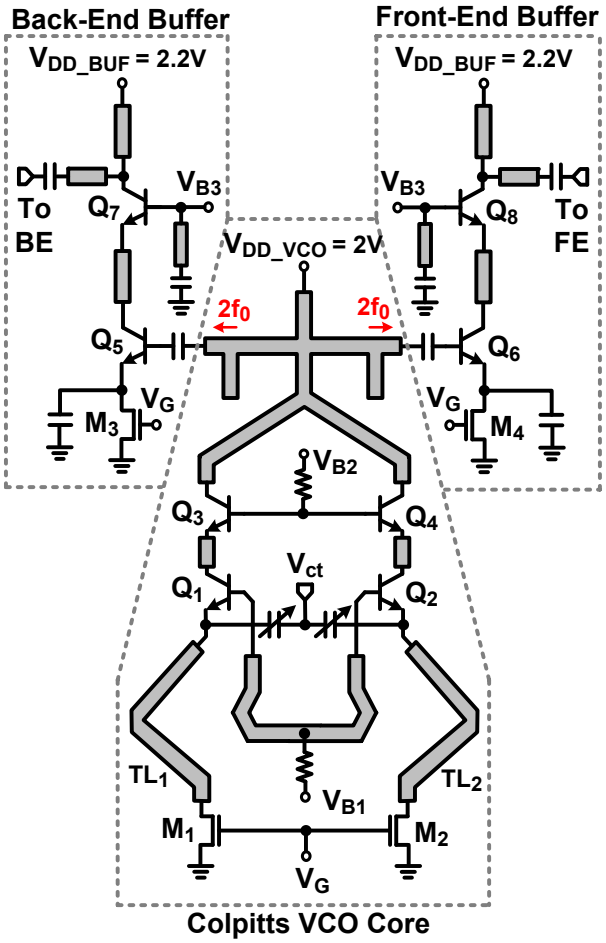


Figure 5.15: Schematic of the VCO as well as the front-end and back-end buffers amplifiers.

5.3.4 Frequency Doubler

As the final stage, the frequency doubler pushes the frequency into the THz band. Schematic of the frequency double used in this design is shown in Fig. 5.16. Since the front-end buffer has a single-end output, a mode-filtering wide-band balun [66] is used to convert it into balanced waves for second harmonic generation in Q_1 and Q_2. In this balun structure, as shown in Fig. 5.17, with excitation on the input line, current flowing on the edges of the gap structure forms return current beneath the output line, which induces differential-mode signal

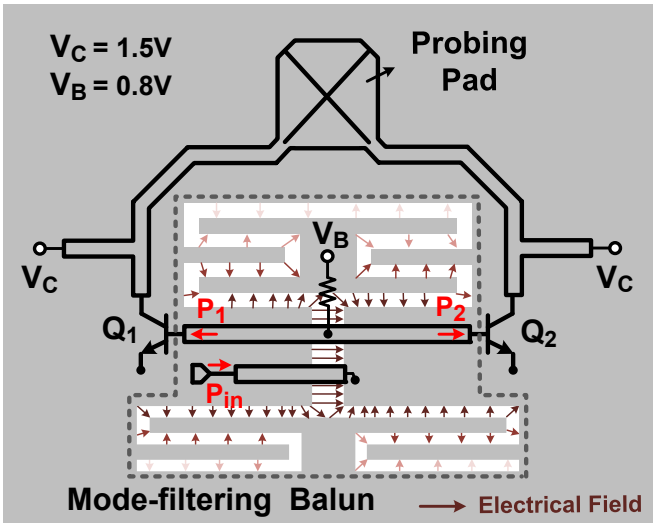


Figure 5.16: Schematic of the frequency doubler.

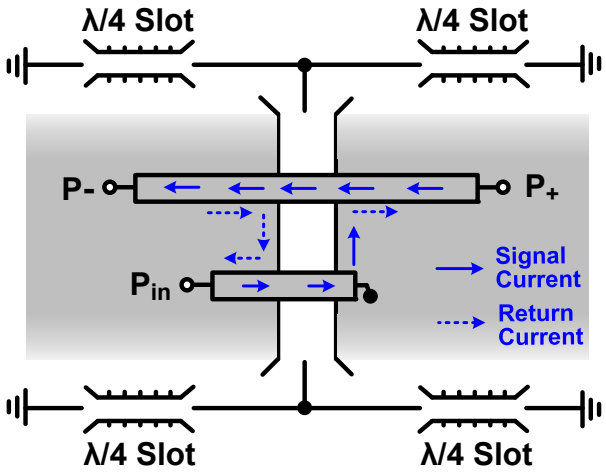


Figure 5.17: The mode filtering slot balun structure.

on the output ports. To support different potentials on the edges of the gap, $\lambda/4$ slots are placed on top and bottom, which are folded to reduce size. Since only differential-mode waves are supported, this balun structure shows negligible phase and amplitude imbalance in a wide bandwidth [66]. The fundamental power is injected from the base of the transistors differentially, and the second harmonic is extracted from the collector. The output probing pad is co-designed

with the frequency doubler and acts as part of the matching network to reduce the signal loss [1].

5.4 Experimental Results

The 316-GHz source prototype is implemented with the STMicroelectronics 0.13-μm SiGe:C BiCMOS process. As shown in Fig. 5.18, the chip occupies an area of 1.0×0.85 mm^2.

To measure the performance of the source, a WR-3 waveguide probe is used to probe the output signal. As shown in Fig. 5.19(a), in the output frequency and spectrum measurement, a VDI WR-3 even-harmonic mixer (EHM) is used to mix the probed output signal with 16^{th} harmonic of an LO (provided by an Agilent signal source) to down-convert it to an IF below 2 GHz. Then, the IF sig-

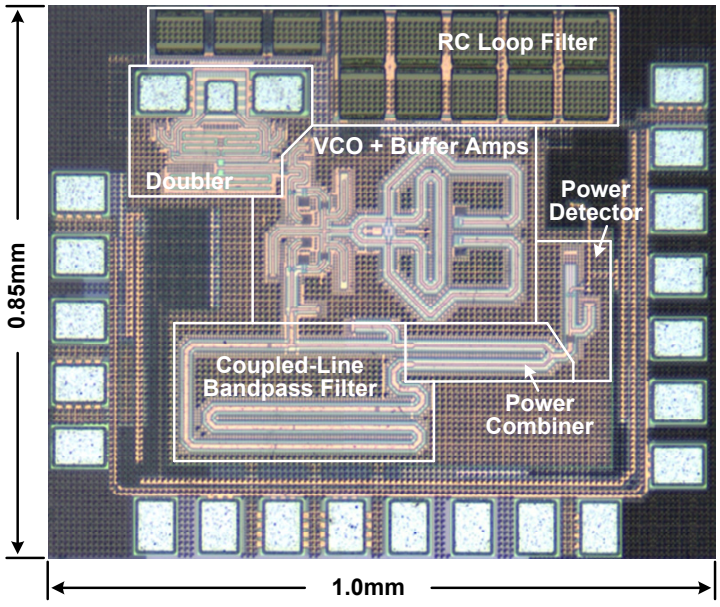
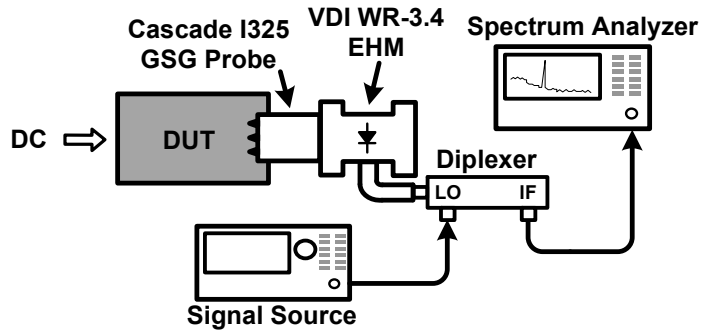
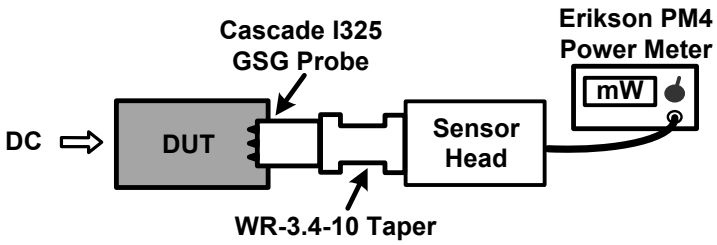


Figure 5.18: Die photograph of the prototype chip.



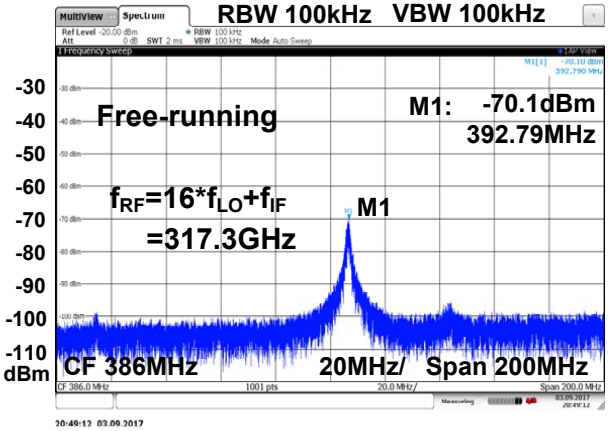
(a)



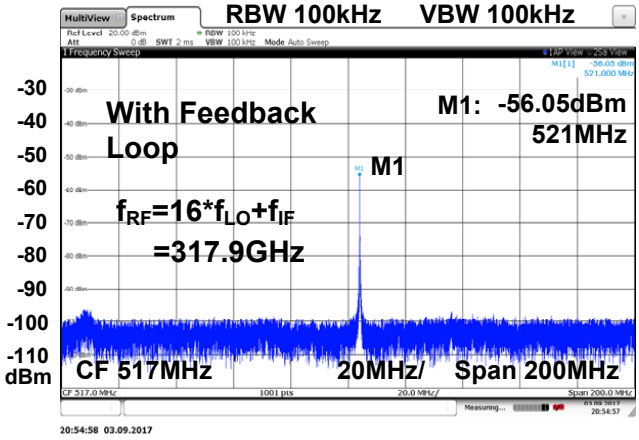
(b)

Figure 5.19: The measurement setups: (a) frequency/spectrum measurement setup and (b) power measurement setup.

nal is measured on a spectrum analyzer. Fig. 5.20 shows the measured down-converted spectrum. When the oscillator is free running, due to supply noise and ambient environment change, frequency drift and large linewidth are observed. With the frequency stabilization feedback loop turned on, a much more stable tone is observed. Phase noise of the output is also measured under both cases, as shown in Fig. 5.21. When the source is free-running, due to frequency drift, the phase noise measurement is only performed down to an offset frequency of 300 kHz. With the feedback loop, the output frequency is stabilized and the phase noise can be measured to a much lower offset frequency. At 100 kHz and 1 MHz offset, the measured phase noise is -72.4 dBc/Hz and -78.5 dBc/Hz, respectively. The simulated phase noise is also plotted in the same figure, which shows a large discrepancy compared to the measurement at offset frequencies from 100 kHz to 1 MHz. This is mainly caused by the fact that the



(a)



(b)

Figure 5.20: The measured output spectrum after down-conversion: (a) free-running and (b) with the frequency stabilization feedback.

implemented responsivity of the power detector differs significantly from the simulation value. Since the simulation relies on the nonlinear behavior of the device at very high frequency, which is very hard to model accurately, the results can be very different compared with measurement. In fact, the measured frequency-to-current gain, $K_{det}\Re_{pd}$, is 139.2 fA/Hz, which is only 61% of the simulated value ($K_{det} \approx 45.5\ fW/Hz$, $\Re_{pd} \approx 5$ A/W in simulation). As shown in Fig. 5.7, a lower frequency-to-current gain causes a smaller system close-loop bandwidth, and consequently, less suppression of the VCO phase noise. Using

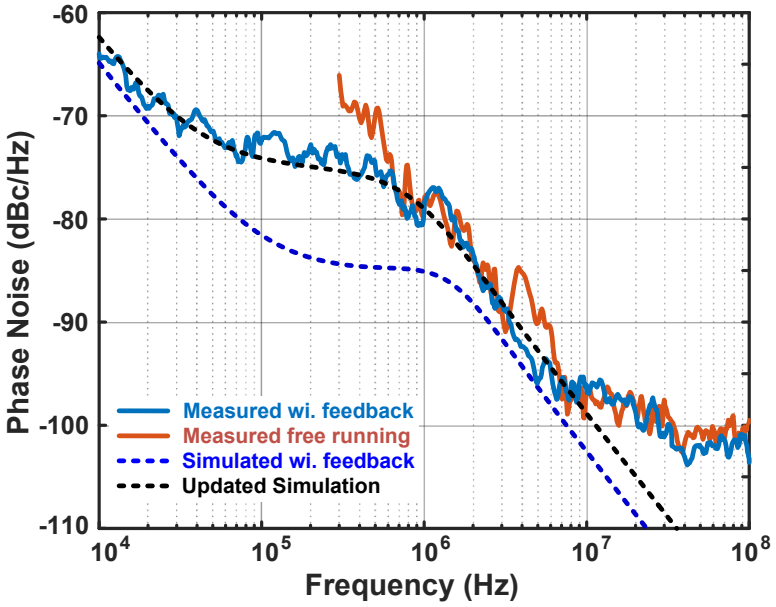


Figure 5.21: The measured and simulated phase noise of the prototype source.

the measured frequency-to-current gain and VCO phase noise data, the total output phase noise simulation result is updated and shown in Fig. 5.7. The resulst now agrees with the measurement well.

To accurately characterize the probed output power of the chip, an Erikson PM4 power meter is used as shown in Fig. 5.19(b). The measured output power within the frequency tuning range is shown in Fig. 5.22. With the VCO tail bias, V_G, changed from 0.5 V to 0.65 V, the total output frequency range achieved is 301.7 to 331.8 GHz, which is around 9.5% with respect to a center frequency of 316 GHz. Within this range, the output power varies from -19.1 to -13.9 dBm, as shown in Fig. 5.22. At different VCO bias points, the total dc power consumption varies from 51.7 to 84.1 mW. The detailed breakdown at the maximum and minimum power consumption cases is shown in Fig. 5.23.

In Table 5.1, performance summaries of the proposed frequency-stabilized

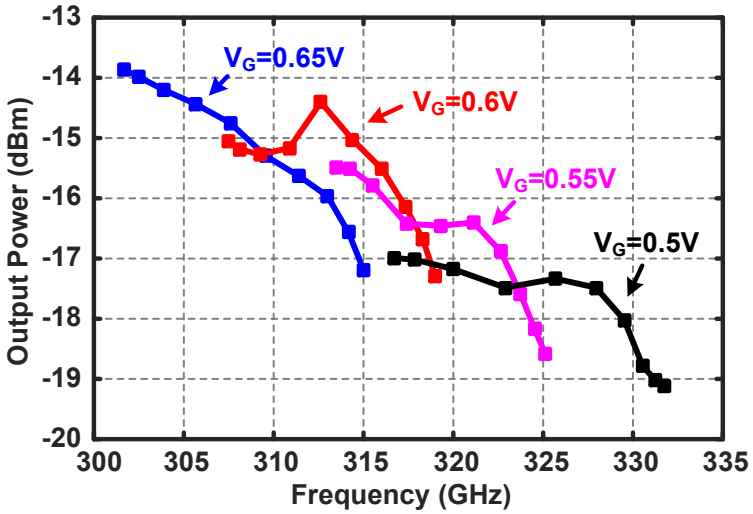


Figure 5.22: The measured output power over the output frequency range.

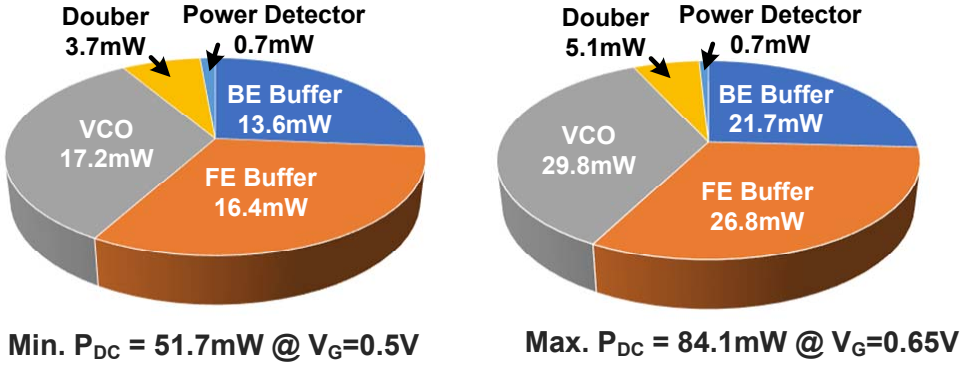


Figure 5.23: The measured dc power consumption breakdown.

source prototype as well as comparison with other state-of-the-art works are given. Thanks to elimination of narrow-band ILFDs and power-consuming ILFD locking range extending schemes, the source demonstrates the largest output frequency range and lowest power consumption while achieving comparable phase noise and output power performances with respect to the state of the art. Due to the small temperature dependence of the dielectric constant of the BEOL insulating layers, the proposed passive reference has a larger temperature coefficient compared to crystal oscillators. However, with significantly

lower system integration cost and power consumption, this scheme is attractive for many applications that require short coherence time, such as short-range mm-wave/THz FMCW radars.

5.5 Conclusion

In this chapter, an entirely-on-chip feedback mechanism for frequency stabilization is described. Based on the inherent frequency response of the on-chip passive EM structures, high-gain frequency detection is achieved without need for any off-chip frequency reference, which can significantly reduce the total system cost. This scheme can also avoid using frequency dividers, which exhibits very narrow-band operation at high frequency. As a result, wider tuning range and much lower dc power consumption is achievable. A 301.7-to-331.8-GHz source prototype is designed with a 0.13-μm SiGe BiCMOS technology, which achieves the largest output frequency range and lowest power consumption with comparable phase noise and output power performances with respect to state of the art according to our measurement.

Table 5.1: Performance summary and comparison.

References	**ISSCC 2015 [2]**	**ISSCC 2014 [70]**	**ISSCC 2016 [71]**	**JSSC 2015 [72]**	**This Work**
Source Type	PLL Inj. Lock. Osc. Array	Osc. + PLL	Osc. + PLL	Inj. Lock. Osc. Chain	Osc. + Freq. Det. Feedback
Frequency (GHz)	317	280~303	539~560	485~511	302~332
Tuning Range	\	7.9%	3.8%	5.1%	9.5%
Frequency Purity	Phase-Locked	Phase-Locked	Phase-Locked	Free-Running	Frequency-Stabilized
Phase Noise @ 100kHz (dBc/Hz)	\	-77.8	-71	\	-72.4
Phase Noise @ 1MHz (dBc/Hz)	-79	-82.5	-74	-87	-78.5
Output Power (dBm)	5.2 † (Radiated)	-14 (Probed)	-27 (Radiated)	-16.6 (Probed)	-13.9 (Probed)
DC Power (mW)	610	376	172	388	51.7
Area (mm^2)	1.6×1.3	1.6×1.6	1.8×1.55	0.72×0.7 (Core)	1×0.85
Technology (f_{max})	130nm BiCMOS (280GHz)	90nm BiCMOS (315GHz)	65nm CMOS (240GHz)	90nm BiCMOS (350GHz)	130nm BiCMOS (280GHz)

† Total power of 16 radiator cells.

CHAPTER 6

CONCLUSIONS

Enabled by fast advancing CMOS and BiCMOS technology scaling, the silicon transistors are becoming more and more powerful for terahertz signal generation and processing. At the same time, huge benefits are brought by silicon integration, such as significantly lower cost and form factor, as well as easy integration with other SoCs to achieve more sophisticated functionalities. As a result, silicon terahertz electronics has a bright future.

In this thesis, high-performance terahertz circuit blocks with new design method as well as novel circuit topology are demonstrated, which achieve great performances. Then, the proposed new circuit blocks are utilized to implement functioning imaging and communication teraherz systems. System level innovations are also proposed to improve the total performances. All the designs demonstrated in this thesis successfully push the state of the art forward, and pave the way for more sophisticated terahertz circuits and systems for future applications, such as portable terahertz imaging devices, terahertz-radar-based driver-assistance systems, high-resolution 3-D terahertz scanning, ultra-high-speed terahertz communication link, as well as high-sensitivity terahertz spectroscopy systems.

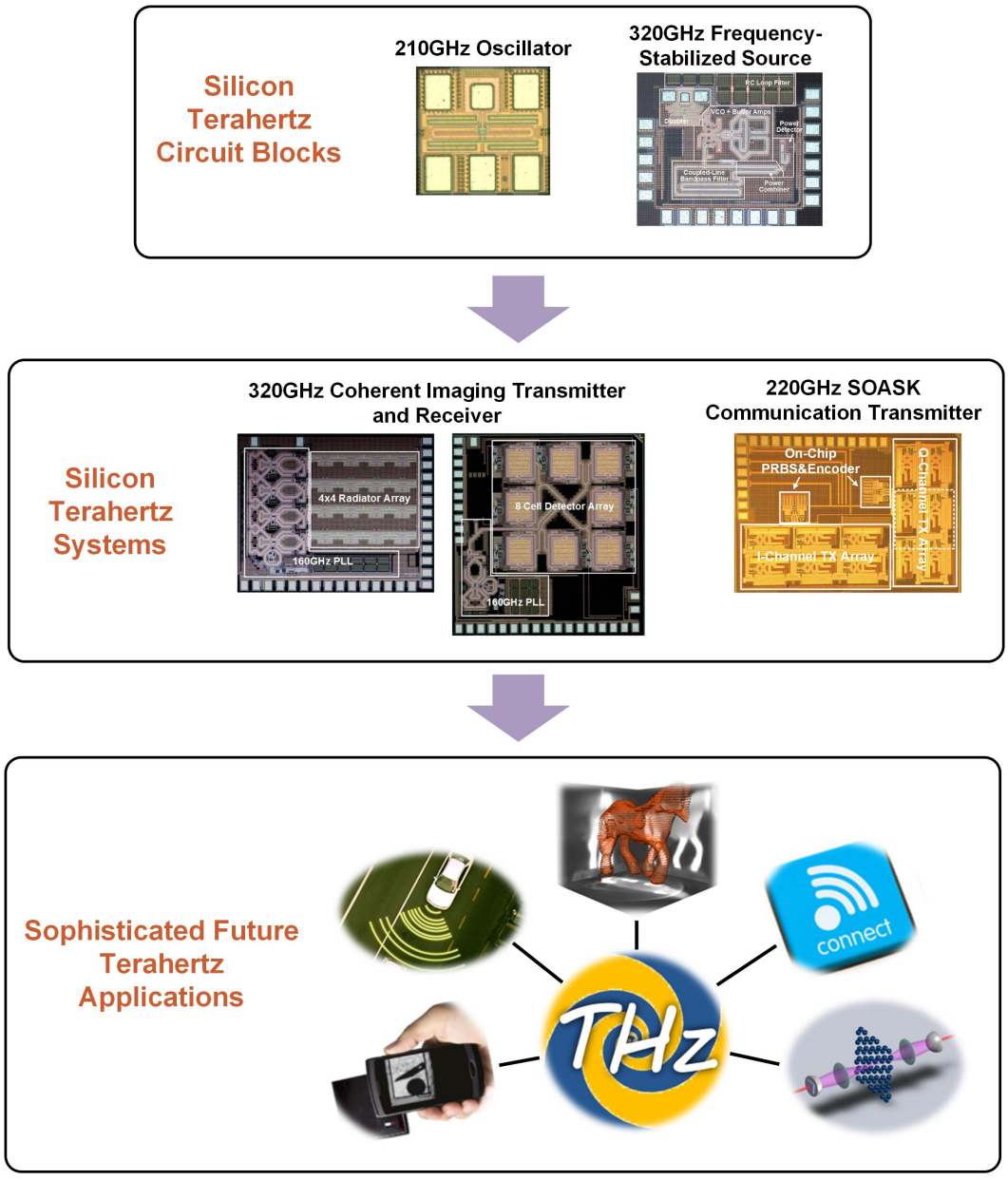


Figure 6.1: Silicon terahertz circuits and systems demonstration in this thesis and potential future applications.

BIBLIOGRAPHY

[1] C. Jiang, A. Cathelin, and E. Afshari, "An efficient 210GHz compact harmonic oscillator with 1.4dBm peak output power and 10.6% tuning range in 130nm BiCMOS," in *IEEE Radio Freq. Integr. Circuits Symp.*, May 2016.

[2] R. Han, C. Jiang, A. Mostajeran, M. Emadi, H. Aghasi, H. Sherry, A. Cathelin, and E. Afshari, "A 320 GHz phase-locked transmitter with 3.3 mW radiated power and 22.5 dBm EIRP for heterodyne THz imaging systems," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 446–447, Feb. 2015.

[3] R. Han, C. Jiang, A. Mostajeran, M. Emadi, H. Aghasi, H. Sherry, A. Cathelin, and E. Afshari, "A SiGe terahertz heterodyne imaging transmitter with 3.3 mw radiated power and fully-integrated phase-locked loop," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2935–2947, Dec. 2015.

[4] C. Jiang, A. Mostajeran, R. Han, M. Emadi, H. Sherry, A. Cathelin, and E. Afshari, "A 320GHz subharmonic-mixing coherent imager in 0.13μm SiGe BiCMOS," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 432–434, Jan. 2016.

[5] C. Jiang, A. Mostajeran, R. Han, M. Emadi, H. Sherry, A. Cathelin, and E. Afshari, "A fully integrated 320 GHz coherent imaging transceiver in 130 nm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2596–2609, Nov. 2016.

[6] R. Han, J. Holloway, C. Jiang, A. Mostajeran, E. Afshari, A. Cathelin, Y. Zhang, K. K. O, L. Boglione, T. Hancock, C. Wang, Z. Hu and G. Zhang, "On-chip terahertz electronics: From device-electromagnetic integration to energy-efficient, large-scale microsystems," *IEEE Int. Electron Devices Meeting*, Dec. 2016.

[7] C. Jiang, A. Cathelin, and E. Afshari, "A high-speed efficient 220 GHz spatial-orthogonal ASK transmitter in 130 nm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2321–2334, Sep. 2017.

[8] C. Jiang, M. Aseeri, A. Cathelin, and E. Afshari, "A 301.7-to-331.8GHz source with entirely on-chip feedback loop for frequency stabilization in 0.13μm BiCMOS," accepted to *IEEE Int. Solid-State Circuits Conf.*, Feb. 2018.

[9] C. Sirtori, "Applied physics: bridge for the terahertz gap," *Nature*, vol. 417, pp. 132133, May 2002.

[10] J. F. Federici, B. Schulkin, F. Huang, D. Gary, R. Barat, F. Oliveira, and D. Zimdars, "THz imaging and sensing for security applications – explosives, weapons and drugs," *Semicond. Sci. Technol.*, vol. 20, no. 7, pp. S266–S280, 2005.

[11] S. J. Oh, Y. M. Huh, S. Haam, J. S. Suh and J. H. Son, "Medical Application of THz Imaging Technique," *IEEE International Conference on Infrared, Millimeter, and Terahertz Waves*, Sep. 2012.

[12] Z. Taylor, R. Singh, D. Bennett, P. Tewari, C. Kealey, N. Bajwa, M. Culjat, A. Stojadinovic, H. Lee, J. Hubschman, E. Brown, and W. Grundfest, "THz medical imaging: in vivo hydration sensing," *IEEE Trans. Terahertz Sci. Technol.*, vol. 1, no. 1, pp. 201–219, Sep. 2011.

[13] J. Grzyb, B. Heinemann, U. R. Pfeiffer, "A fully integrated 0.55THz near-field sensor with a lateral resolution down to 8m in 0.13m SiGe BiCMOS," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 424–425, Jan. 2016.

[14] T. Globus, D. Woolard, T. W. Crowe, T. Khromova, B. Gelmont, and J. Hesler, "Terahertz fourier transform characterization of biological materials in a liquid phase," *J. Phys. D: Appl. Phys.*, vol. 39, no. 15, pp. 3405–3413, 2006.

[15] P. H. Siegel, "Terahertz Technology," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 910–928, Mar. 2002.

[16] H. Hoshina, "Molecular spectroscopy by a Terahertz Time Domain Spectrometer," *Online.*

[17] Q. Zhong, W. Choi, C. Miller, R. Henderson and K. K. O "A 210-to-305GHz CMOS Receiver for Rotational Spectroscopy," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 426–427, Jan. 2016.

[18] M. Naftaly and R. E. Miles, "Terahertz time-domain spectroscopy for material characterization," *Proceedings of the IEEE*, vol. 95, no. 8, pp. 1658–1665, Aug. 2007.

[19] I. R. Medvedev, C. F. Neese, G. M. Plummer and F. C. De Lucia, "Submillimeter spectroscopy for chemical analysiswith absolute specicity," *Optics Letters*, vol. 35, no. 10, pp. 1533–1535, May 2010.

[20] "Astronomical spectroscopy," *Wikipedia, Online.*

[21] J. Federici and L. Moeller, "Review of terahertz and subterahertz wireless communications," *J. Applied Physics*, vol. 107, no. 11, 2010.

[22] R. Han, "Holistic design approach for terahertz electronics: from devices to systems," *PhD Thesis*, Cornell University, 2014.

[23] R. Spence, *Linear Active Networks,* Wiley-Interscience, New York, 1970.

[24] R. Han, Y. Zhang, Y. Kim, D. Y. Kim, H. Shichijo, E. Afshari, and K. Kenneth, "Active terahertz imaging using schottky diodes in CMOS: Array and 860-GHz pixel," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2296-2308, Oct. 2013.

[25] R. Al Hadi, H. Sherry, J. Grzyb, Y. Zhao, W. Forster, H. Keller, A. Cathelin, A. Kaiser, and U. Pfeiffer, "A 1 k-pixel video camera for 0.7–1.1 terahertz imaging applications in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, pp. 2999–3012, Dec 2012.

[26] M. Uzunkol, O. Gurbuz, F. Golcuk, and G. Rebeiz, "A 0.32 THz SiGe 4x4 imaging array using high-efficiency on-chip antennas," *IEEE J. Solid-State Circuits*, vol. 48, pp. 2056–2066, Sept 2013.

[27] S. Kang, S. V. Thyagarajan and A. M. Niknejad, "A 240 GHz fully integrated wideband QPSK transmitter in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2256-2267, Oct. 2015.

[28] S. V. Thyagarajan, S. Kang and A. M. Niknejad, "A 240 GHz Fully Integrated Wideband QPSK Receiver in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2268-2280, Oct. 2015.

[29] E. Afshari and R. Han, "Progress towards mW-power generation in CMOS THz signal sources," in *European Microwave Integrated Circuits Conference (EuMIC)*, pp. 117–120, Oct. 2013.

[30] O. Momeni and E. Afshari, "High power terahertz and millimeter-wave oscillator design: a systematic approach," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 583-597, Mar. 2011.

[31] K. Sengupta and A. Hajimiri, "A 0.28 THz power-generation and beam-steering array in CMOS based on distributed active radiators," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3013–3031, Dec. 2012.

[32] J. Grzyb, Y. Zhao, and U. Pfeiffer, "A 288-GHz lens-integrated balanced triple-push source in a 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1751–1761, Jul. 2013.

[33] M. Adnan and E. Afshari, "A 247-to-263.5GHz VCO with 2.6mW peak output power and 1.14% DC-to-RF efficiency in 65nm bulk CMOS," *ISSCC Dig. Tech. Papers*, pp. 262–263, Feb. 2014.

[34] Y. M. Tousi, O. Momeni and E. Afshari, "A novel CMOS high-power terahertz VCO based on coupled oscillators: theory and implementation," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3032–3042, Dec. 2012.

[35] P. Chiang, O. Momeni and P. Heydari, "A 200-GHz inductively tuned VCO with -7-dBm output power in 130-nm SiGe BiCMOS," *IEEE Trans. Microw. Theory Technol.*, vol. 61, pp. 3666–3673, Oct. 2013.

[36] R. Kananizadeh and O. Momeni, "A 190.5GHz mode-switching VCO with 20.7% continuous tuning range and maximum power of -2.1dBm in 0.13μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 52–53, Feb. 2016.

[37] R. Han and E. Afshari, "A CMOS high-power broadband 260-GHz radiator array for spectroscopy," *IEEE J. Solid-State Circuits*, vol. 48, pp. 3090–3104, Dec. 2013.

[38] D. Ham and A. Hajimiri, "Concepts and methods in optimization of integrated LC VCOs," *IEEE J. Solid-State Circuits*, vol. 36, no. 6, pp. 896–909, Jun. 2001.

[39] S. Jameson and E. Socher, "High efficiency 293 GHz radiating source in 65 nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 7, pp. 463–465, Jul. 2014.

[40] S. P. Voinigescu, A. Tomkins, E. Dacquay, P. Chevalier, J. Hasch, A. Chantre, and B. Sautreuil, "A study of SiGe HBT signal sources in the 220-330-GHz range, *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 20112021, Sep. 2013.

[41] G. B. Rybicki and A. P. Lightman, *Radiative Processes in Astrophysics*. John Wiley & Sons., 1979.

[42] Y. Tousi and E. Afshari, "A high-power and scalable 2-D phased array for terahertz CMOS integrated systems," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 597–609, Feb. 2015.

[43] U. Pfeiffer, Y. Zhao, J. Grzyb, R. Al Hadi, N. Sarmah, W. Forster, H. Rucker, and B. Heinemann, "A 0.53 THz reconfigurable source module with up to 1 mW radiated power for diffuse illumination in terahertz imaging applications," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2938–2950, Dec. 2014.

[44] F. Friederich, W. von Spiegel, M. Bauer, F. Meng, M. Thomson, S. Boppel, A. Lisauskas, B. Hils, V. Krozer, A. Keil, T. Loffler, R. Henneberger, A. Huhn, G. Spickermann, P. Bolivar, and H. Roskos, "THz active imaging systems with real-time capabilities," *IEEE Trans. Terahertz Sci. Technol.*, vol. 1, no. 9, pp. 183–200, Sep. 2011.

[45] P.-Y. Chiang, Z. Wang, O. Momeni, and P. Heydari, "A silicon-based 0.3 THz frequency synthesizer with wide locking range," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2951–2963, Dec. 2014.

[46] K. Statnikov, J. Grzyb, B. Heinemann, and U. R. Pfeiffer, "160-GHz to 1-THz multi-color active imaging with a lens-coupled SiGe HBT chip-set," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 520–532, Feb. 2015.

[47] A. Siligaris, Y. Andee, E. Mercier, J. M. Guerra, J. F. Lampin, G. Ducournau, and Y. Quere, "A 278 GHz heterodyne receiver with on-chip antenna for THz imaging in 65 nm CMOS process," in *European Solid-State Circuits Conf. (ESSCIRC)*, pp. 307–310, Sep. 2015.

[48] K. Sengupta, D. Seo, L. Yang, and A. Hajimiri, "Silicon integrated 280 GHz imaging chipset with 4×4 SiGe receiver array and CMOS source," *IEEE Trans. Terahertz Sci. Technol.*, vol. 5, no. 5, pp. 427–437, May 2015.

[49] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

[50] P. Chevalier, T. Lacave, E. Canderle, A. Pottrain, Y. Carminati, J. Rosa, F. Pourchon, N. Derrier, G. Avenier, A. Montagne, A. Balteanu, E. Dacquay, I. Sarkas, D. Celi, D. Gloria, C. Gaquiere, S. Voinigescu, and A. Chantre, "Scaling of SiGe BiCMOS technologies for applications above 100 GHz," in *Proc. IEEE Compound Semiconductor Integrated Circuit Symp.*, pp. 1–4, Oct. 2012.

[51] A. Mirzaei, M. E. Heidari, R. Bagheri, and A. A. Abidi, "Multi-phase injection widens lock range of ring-oscillator-based frequency dividers," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 656–671, Mar. 2008.

[52] R. Han, Y. Zhang, D. Coquillat, H. Videlier, W. Knap, E. Brown, and K. O, "A 280-GHz schottky diode detector in 130-nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2602–2612, Nov. 2011.

[53] Z. Wang, P. Y. Chiang, P. Nazari, C. C. Wang, Z. Chen, and P. Heydari, "A CMOS 210-GHz fundamental transceiver with OOK modulation," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 564–580, Mar. 2014.

[54] K. Katayama, K. Takano, S. Amakawa, S. Hara, A. Kasamatsu, K. Mizuno, K. Takahashi, T. Yoshida, and M. Fujishima, "A 300GHz 40nm CMOS transmitter with 32-QAM 17.5Gb/s/ch capability over 6 channels," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 342–343, Jan. 2016.

[55] J. D. Jackson, *Classical Electrodynamics Third Edition*. John Wiley, 1979.

[56] S. Haykin, *Digital Communications*. John Wiley & Sons, 1998.

[57] J. F. Wakerly, *Digital Design: Principles & Practices*. New Jersey, USA: Prentice Hall, 1994.

[58] D. M. Pozar, *Microwave Engineering*. New York, USA: John Wiley & Sons, 2005.

[59] T. Hirota, A. Minakawa, and M. Muraguchi, "Reduced-size branch-line and rat-race hybrids for uniplanar MMIC's," *IEEE Trans. Microw. Theory Tech.*, vol. 38, pp. 270–275, Mar. 1990.

[60] *Nominal Horn Specification*. Charlottesville, VA, USA: Virginia Diodes Inc., 2016.

[61] C. A. Balanis, *Antenna Theory: Analysis and Design*. Wiley, 2015.

[62] H. T. Friis, "A note on a simple transmission formula," *Proceedings of the IRE*, vol. 34, pp. 254–256, May 1946.

[63] *WR5.1ZBD-F User Guide*. Charlottesville, VA, USA: Virginia Diodes Inc., 2016.

[64] *Agilent 83483A,4A,4B and 54751A,2A,2B Plug-In Modules Users Guide*. Santa Clara, CA, USA: Agilent Technologies, 2000.

[65] B. Razavi, *RF Microelectronics 2nd Edition*. Prentice Hall, 2011.

[66] C. Wang and R. Han, "Rapid and energy-efficient molecular sensing using dual mm-wave combs in 65nm CMOS: A 220-to-320GHz spectrometer with 5.2mW radiated power and 14.6-to-19.5dB noise figure," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 302–303, Feb. 2017.

[67] A. Lacaita, S. Levantino and C. Samori, *Integrated Frequency Synthesizers for Wireless Systems*, New York: Cambridge University Press, 2007.

[68] S. Levantino, L. Collamati, C. Samori and A. Lacaita, "Folding of phase noise spectra in charge-pump phase-locked loops induced by frequency division", *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 9, pp. 671–675, Sep. 2010.

[69] D. M. Pozar, *Microwave Engineering, Third Edition*, New York: John Wiley & Sons, Inc., 2005.

[70] P. Chiang et al., "A 300GHz frequency synthesizer with 7.9% locking range in 90nm SiGe BiCMOS," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 260-261, Feb. 2014.

[71] Y. Zhao, Z. Chen, G. Virbila, Y. Xu et al., "An integrated 0.56THz frequency synthesizer with 21GHz locking range and -74dBc/Hz phase noise at 1MHz offset in 65nm CMOS," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 36–37, Feb. 2016.

[72] T. Chi, J. Luo, S. Hu and H. Wang, "A multi-phase sub-harmonic injection locking technique for bandwidth extension in silicon-based THz signal generation," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1861-1873, Aug. 2015.

[73] H. J. Song, J. Y. Kim, K. Ajito, N. Kukutsu, and M. Yaita, "50-Gb/s direct conversion QPSK modulator and demodulator MMICs for terahertz communications at 300 GHz," *IEEE Trans. Microw. Theory Tech.*, vol. 62, pp. 600–609, Mar. 2014.

[74] Y. Ye, B. Yu and Q. Gu, "A 165-GHz transmitter with 10.6% peak DC-to-RF efficiency and 0.68-pJ/b energy efficiency in 65-nm bulk CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 64, pp. 4573–4584, Dec. 2016.

[75] N. Sarmah, J. Grzyb, K. Statnikov, S. Malz, P. R. Vazquez, W. Ferster, B. Heinemann, and U. R. Pfeiffer, "A fully integrated 240-GHz direct-conversion quadrature transmitter and receiver chipset in SiGe technology," *IEEE Trans. Microw. Theory Tech.*, vol. 64, pp. 562–574, Feb. 2016.

[76] J. D. Park, S. Kang, S. V. Thyagarajan, E. Alon, and A. M. Niknejad, "A 260 GHz fully integrated CMOS transceiver for wireless chip-to-chip communication," *IEEE Symposium on VLSI Circuits (VLSIC)*, pp. 48–49, Jun. 2012.

[77] S. Jameson, E. Halpern and E. Socher, "A 300GHz wirelessly locked 2×3 array radiating 5.4dBm with 5.1% DC-to-RF efficiency in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 348–349, Feb. 2016.

[78] M. Elkhouly, Y. Mao, C. Meliani, F. Ellinger, and C. Schyett, "A 245 GHz ASK modulator and demodulator with 40 Gbits/sec data rate in 0.13 μm SiGe BiCMOS technology," *IEEE International Microwave Symposium (IMS)*, pp. 1–3, Jun. 2013.

[79] *High Frequency Structure Simulator (HFSS) User Guide*, ANSYS Inc. [Online]. Available: http://www.ansys.com/.

[80] H. Khatibi, S. Khiyabani and E. Afshari, "A 173 GHz amplifier with a 18.5 dB power gain in a 130 nm SiGe process: a systematic design of high-gain amplifiers above $f_{max}/2$," accepted to *IEEE Trans. Microw. Theory Tech.*, 2017.

[81] S. Orfanidis, *Introduction to Signal Processing*, New Jersey: Pearson Education, Inc., 2009.

[82] S. Orfanidis, *Electromagnetic Waves and Antennas*, [Online]. Available: http://www.ece.rutgers.edu/~orfanidi/ewa/.

[83] B. Cetinoneri, Y. Atesal, A. Fung and G. Rebeiz, "W-band amplifiers with 6-dB noise figure and milliwatt-level 170-200-GHz doublers in 45-nm CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 60, pp. 692–701, Mar. 2012.

[84] O. Momeni, "A 260GHz amplifier with 9.2dB gain and -3.9dBm saturated power in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 140–141, Feb. 2013.

[85] X. Wu, K. Sengupta, "Dynamic waveform shaping with picosecond time widths," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 389-405, Feb. 2017.

[86] H. Bameri and O. Momeni, "A high-gain mm-wave amplifier design : an analytical approach to power gain boosting," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 357-370, Feb. 2017.

[87] X. Gao, Eric A. M. Klumperink, M. Bohsali and B. Nauta, "A low noise subsampling PLL in which divider noise is eliminated and PD/CP noise is not

multiplied by N^2," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3253-3263, Dec. 2009.

[88] A. Niknejad and H. Hashemi, *mm-Wave Silicon Technology 60 GHz and Beyond*, Springer, 2008.

[89] M. Adnan and E. Afshari, "A 105-GHz VCO with 9.5% tuning range and 2.8-mW peak output power in a 65-nm bulk CMOS process," *IEEE Trans. Microw. Theory Tech.*, vol. 62, pp. 753–762, Apr. 2014.

[90] R. Han and E. Afshari, "A high-power broadband passive terahertz frequency doubler in CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 61, pp. 1150–1160, Mar. 2013.

[91] S. M. Bowers, A. Safaripour, and A. Hajimiri, "Dynamic polarization control," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1224-1236, May. 2015.

[92] J. Lee, M. Kim, and K. Yang, "A 1.52 THz RTD triple-push oscillator with a μW-level output power," *IEEE Trans. THz Sci. Technol.*, vol. 6, pp. 336–340, Mar. 2016.